Study and modelling of the disturbances produced within the STM32 microcontrollers under pulsed stresses

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Thèse de doctorat

Présentée en vue de l'obtention du
grade de docteur en Sciences spécialité Electronique

par

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Etude et modélisation des perturbations produites au sein des microcontrôleurs STM32 soumis à des stress en impulsion

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Soutenance prévue le 27 Avril 2017

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Acronym list

AC: Alternating Current

ADC: Analog to Digital Converter

CDM: Chip Discharge Model

CMOS: Complementary Metal Oxyde Semiconductor

CPU: Central Processing Unit

DAC: Digital to Analog Converter

DC: Direct Current

DIP: Dual Inline Package

DUT: Device Under Test

EEPROM: Electrically-Erasable Programmable Read Only Memoy

EFT: Electrical Fast Transient

EMC: ElectroMagnetic Compatibility

EMC: electromagnetic compatibility

EMS: ElectroMagnetic Susceptibility

ESD: ElectroStatic Discharge

FTB : Fast Transient Burst

FTB_{th-} : Fast Transient Burst negative robustness threshold

FTB_{th+} : Fast Transient Burst positive robustness threshold

GND: (GrouND) Used to describe the global perfect reference node

GTEM Cell: Gigahertz Transverse ElectroMagnetic Cell

HBM: Human Body Model

HF: High Frequency

IB: Immunity Behavior

IC: Integrated Circuit

ICEM: Integrated Circuit Emission Model

ICIM: Integrated Circuit Immunity Model

IEC: International Electrotechnical Commission

IO: Input/Output

IP: Intelectual Properties

LF: Low Frequency

MCU: Microcontroller unit

MCU: MicroController Unit

PCB: Printed Circuit Board

PDN: Passive Distribution Network or Power Delivery Network

QFP100: Quad Flat Package 100 pins

RAM: Random Access Memory

RLC: Used to describe circuit composed by resistor inductor and capacitor.

ROM: Read Only Memory

SMA: SubMiniature version A (used for connectors)

SMB: SubMiniature version B (used for connectors)

SMD: Surface mounted device

SOC: System On Chip

SPICE: Simulation Program with Integrated Circuit Emphasis

TEM Cell : Transverse ElectroMagnetic Cell

VDD: (Voltage Drain Drain) Used to describe the local power node

VSS: (Voltage Source Source) Used to describe the local reference node

Introduction

This PhD work takes place in the Microcontroller Division of STMicroelectronics Company in partnership with EpOC laboratory, University of Nice Sophia Antipolis, and financed by the ANRT (Association Nationale Recherche Technologie). This work was done in the team responsible of IO development and Electromagnetic compatibility.

The robustness of products is a key to be distinguished in the competitive market of microcontrollers. A first thesis was made in the team regarding Electro Magnetic Interaction (EMI) by Jean Pierre LECA [1]. The aim of these researches was to create a reusable model to forecast EMI behavior of microcontrollers. Moreover this model permits also to find the weakness of a product and is proved to be very useful to improve performances. It is in the same context of continuous improvement, but this time on EMC susceptibility, that this new PhD work takes place.

Lot of work was done on Electro Static Discharge (ESD) to protect chips from physical damages [2]. It permits to create ESD protections and decrease losses during the manufacturing (Chip Discharge Model, CDM protections) and handling processes (Human Body Model, HBM protection). But ESD and more generally fast transient disturbance can occur during all the microcontroller's life, and cause functional failures.

Studies on behavior of microcontrollers during fast transient are rare, whereas standard like functional ESD IEC 61000-4-2 [3] or FTB (Fast Transient Burst) standard IEC61000-4-4 [4] are references in EMC product evaluation. Physical ESD protections still work when the microcontroller is running and absorb a part of the stress but can't prevent from disturbance on supply and signals.

Microcontrollers are composed by several sub-circuits which can be susceptible to disturbances. The environment (package, PCB) is also influent

parameters on robustness. Indeed it was observed that a sub-circuit integrated on different microcontrollers can be susceptible in one and not in the other. This work will focus on the study of the FTB test. Currently, concerning this test, the influence of such parameters are observed but not understood. Moreover, when a failure happens no measurement is possible to find the cause.

The aim of this thesis work is to understand the FTB stress propagation mechanisms and give tools to analyze failures and find ways to improve robustness. To achieve this, the manuscript is organized in 4 chapters.

The first one presents the context of this study and introduces the problematic. After a presentation of what is a microcontroller and its application field, an overview of the electrical test flow will leads to the presentation of the core of this work: the FTB test. To finish, measurement issues and the state of the art which are the reason of this work will be introduced.

The second chapter is dedicated to the FTB stress propagation mechanisms. Firstly the influence of the supply network will be studied. Results of this study will be used as a basis for the stress propagation understanding. It will lead to the formulation of a hypothesis which will be verified in the FTB test conditions.

In the chapter 3 power network analysis methods will be developed thanks to the understanding of the stress propagation. Based on resonance phenomenon, those tools will be presented and then compared to give a complete toolbox for chip analysis.

In the chapter 4 the contribution of this thesis work will be used with the objective of robustness improvement. The stress propagation understanding and tools will help to identify weakness of microcontrollers and keys to improve their robustness. To finish, perspectives opened by this work will be presented.

Chapter 1 Problematic introduction and state of the art

1 Microcontroller

A microcontroller (MCU), depicted in Figure 1, is a complex System on Chip (SoC) which integrates on a single Integrated Circuit (IC), a processor core (Control Process Unit, CPU), memories (EEPROM, FLASH, and RAM), analog IPs and lot of Inputs/Outputs (IOs) [5]. The advantage of a microcontroller is that it reduces the size and the cost of a user application that uses microprocessor, memories and IOs separately. MCU are designed for embedded applications. Although they are designed in less aggressive technologies than microprocessors and working at lower frequencies.

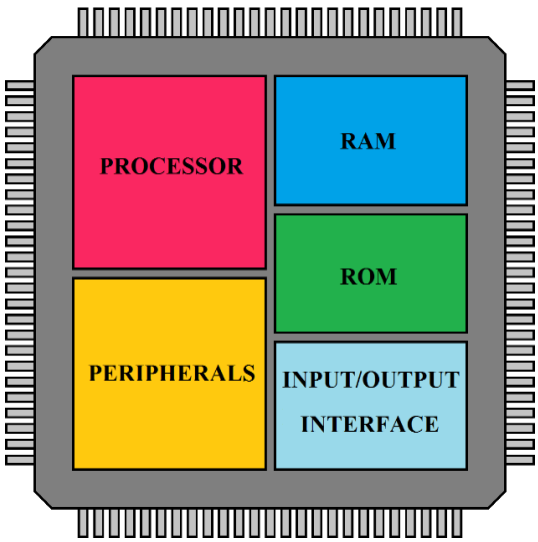


Figure 1: Microcontroller schematic

The design of such system involves lot of core business. The main ones are Analogic, digital, IO and SOC design. Analog designers work mainly on peripherals (ADC, DAC, …) and supply regulation and monitoring. Digital designers work on processor, internal and external communication features. IO

designers design the interface between the chip core and external pin including protection of the chip against external stresses. SOC designers are in charge of assembling all parts.

A microcontroller is a programmable chip and can be used in a wide application range. It is used for instance in washing machines, cell phones, medical, automotive, industry, robotic and so forth. To meet the market demand, several families of microcontrollers are developed. The Figure 2 shows STMicroelectronics microcontrollers' families and their particularities. This study will focus mainly on STM32FX families which are made for mainstream and high performance applications. Those families contain 32 bit microcontrollers based on ARM Cortex cores. They are made with 180nm to 40nm technology nodes. Some products are still under development and many are already on the market.

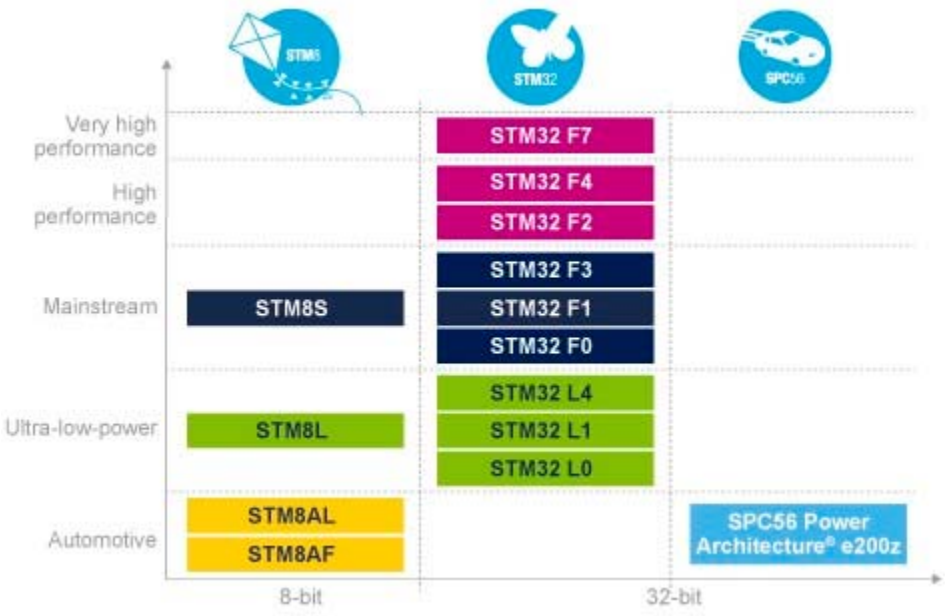


Figure 2: ST microcontroller's families [6]

To be a multi-application device implies to be compatible with all environment constraints. Humidity, temperature but also electromagnetic interferences are part of it. By this way, microcontrollers support several communication standards, a wide temperature range, and harsh electromagnetic environments. An electrical stress test flow is applied on products to evaluate their robustness performance.

2 Microcontroller electrical stress test flow

To guarantee their robustness to electrical stress, microcontrollers are submitted to physical robustness test before functional EMC (ElectroMagnetic Compatibility) evaluation like illustrated in Figure 3. The Physical robustness test flow includes ESD like HBM (Human Body Model) [7], CDM (Chip Discharge Model) [8] and Latchup [9] tests. Those tests allow to know the limit beyond which the chip is subject to physical damages. If there is an abnormal robustness threshold at this step of the test flow, the microcontroller is modified for improvement by designers and has to be manufactured again.

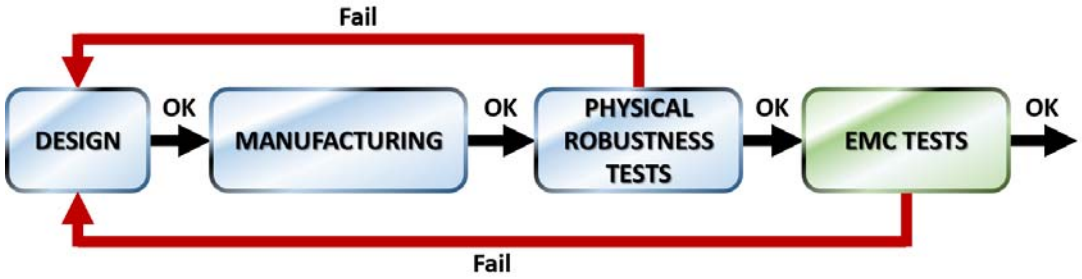


Figure 3: Electrical stress test flow

EMC tests are performed while the microcontroller is executing a normal activity representative program. During tests, the correct behavior of the microcontroller is checked when it is submitted to different kind of stress. EMC tests take place after physical robustness evaluations so no physical damages are expected during this step. EMC tests are also made to verify that the chip does not disturb its environment. As well as the physical robustness tests, if an abnormal robustness or emission threshold is detected, the microcontroller returns to the design step for correction. The EMC topic is developed in the next part.

2.1 Physical robustness tests and protections

2.1.1 HBM (Human Body Model)

During its movements, the human body accumulates charges by triboelectric effect [10]. By this way the body capacitance charges itself positively or negatively. When a person touches an object, his electrical potential can be different from the object and will be equilibrated by the capacitance discharge through the resistance of the body. The potential difference can reach several kV and the current several amps during a very short time.

2.1.1.1 HBM test description

The HBM test is compliant with the ANSI/ESDA/JEDEC JS-001-2010 standard [7]. This test simulates the discharge of a human body in device pins to simulate an ESD during a handling. The ESD simulator reproduces the capacitance and the resistance of a human body with a 100pF capacitance which is discharged through a 1.5kΩ resistance. The schematic diagram of the ESD simulator is represented in Figure 4 with the current waveform in a shorting wire.

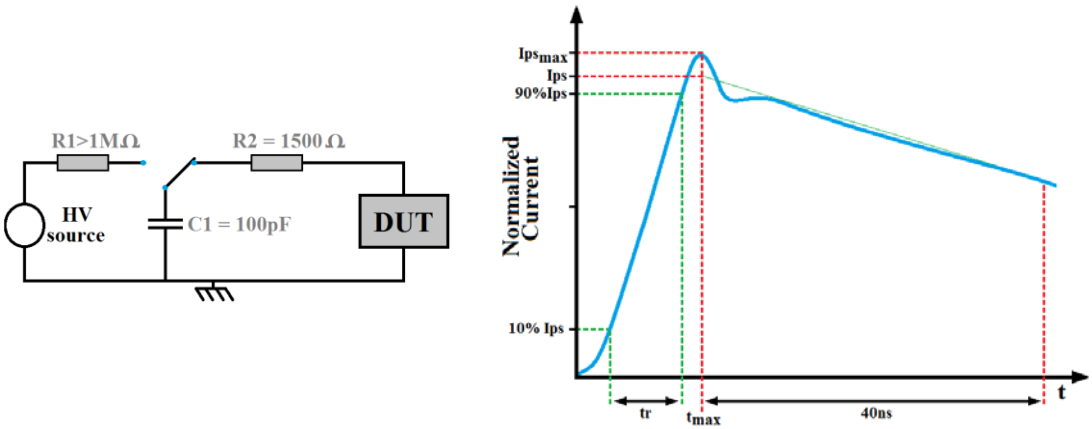


Figure 4: HBM schematic diagram and current waveform in a shorting wire

The current waveform depends on the load but the generator is calibrated by applying the discharge in a short circuit and normalized loads. During the test, a discharge is applied between each pin of the tested device. Each pin is tested with respect to all others for different voltage levels which

reach several kV. If a physical damage is observed for a voltage below the maximum test limit, this voltage is considered as the robustness threshold. If no damage is observed until the maximum test voltage, the maximum voltage is written in the datasheet.

2.1.1.2 ESD clamp protection

When an ESD occurs, the capacitance is discharged from the higher potential to the lower through the chip. To protect circuits, the ESD current must flow from one pin to the other without damaging internal components. To avoid overvoltage and keep local voltage below the maximum supported by components, ESD clamp protections are implemented. Those protections have trigger voltage above maximum supply voltage but below circuit robustness limit. When this device is triggered, a low impedance path is created in parallel with the protected circuit and limits the peak voltage.

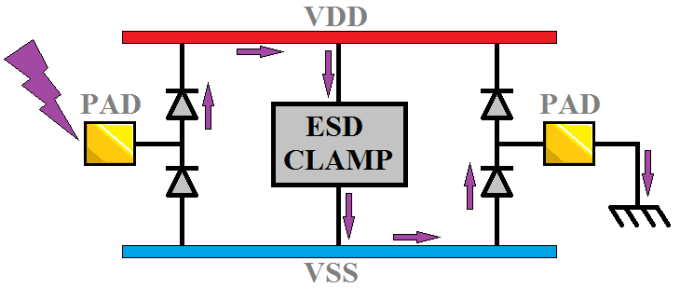


Figure 5: ESD protection principle (positive stress)

Diodes are placed on each pad which need to be protected and the ESD clamp system can be common to several or implemented in each IO, as shown in Figure 5. Diodes guide the current to the ESD Clamp protection. Notice that during handling the supply is not present.

2.1.2 CDM (Chip Discharge Model)

During manufacturing a chip is exposed to electrical fields and accumulates charges. Consequently when a pin is in contact with another electric potential a charge transfer happens. Discharge paths are different from HBM test. Other fails not covered by the previous test can be discovered and by this way, specific protections are also implemented.

2.1.2.1 CDM test description

The JEDEC standard JESD22-C101E [8] describes the chip discharge model test which is applied on microcontrollers. This time, the chip is charged by an electric field positively or negatively and discharged in a ground plane. The Figure 6 represents the test bench principle and the stress current waveform in normalized condition extracted from the standard. The Table 1 synthetizes test parameters.

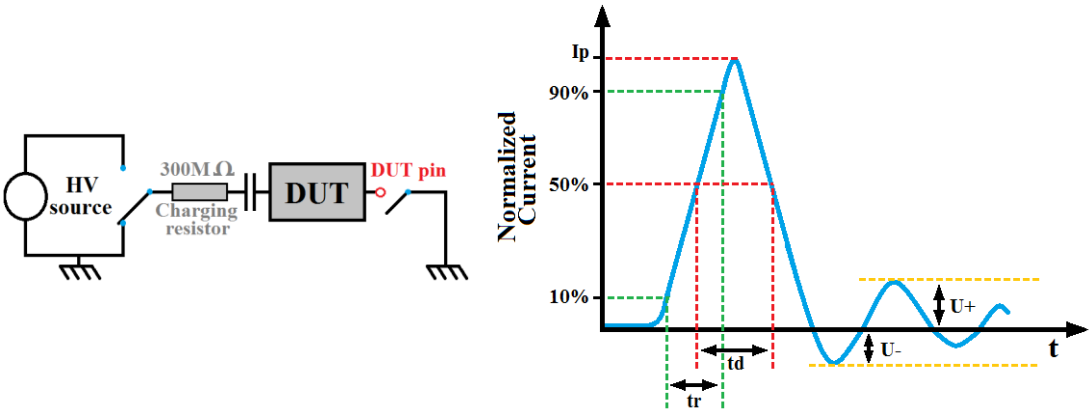


Figure 6: CDM principle and current waveform for positive polarity

Table 1: Test parameters

		Test Number			
		#1	#2	#3	#4
Standard test module		**Small**	**Small**	**Large**	**Large**
Test Voltage (V)		500 (±5%)	1000 (±5%)	200 (±5%)	500 (±5%)
Peak current Magnitude (A)	Ip	5.75 (±15%)	11.5 (±15%)	4.5 (±15%)	11.5 (±15%)
Rise time (ps)	Tr	<400	<400	-	-
Full width at half height (ns)	Td	1.0 (±0.5)	1.0 (±0.5)	-	-
Undershoot (A,max)	U-	<50% Ip	<50% Ip	<50% Ip	<50% Ip
Overshoot	U+	<25% Ip	<25% Ip	<25% Ip	<25% Ip

2.1.2.2 CDM protections

In the CDM case, the chip discharges itself through a pin. Whereas in the ESD HBM stress, two pins are involved, and the discharge current paths is managed thanks to the IO ESD network. During the ESD CDM stress, any internal wall (substrate p, isolated pwell, nwell) will accumulate loads and will have to find a discharge path to any contacted pin. As a consequence, the risk

is located internally in the die, in a place where no ESD network is built. In this case, the main risk is that the best path for the current passes through transistor grid and breaks oxide or through any weak component. The principle of protection is to create preferential path for the current from internal accumulation area to pins.

2.1.3 Latchup

The latchup is a phenomenon due to parasitic NPNP structures in the silicon. Those structures can be triggered by over or under voltages on pins or supplies and create a very low impedance path between VDD and GND which can be hold. The latchup is responsible of functionality fails, over consumption or even physical damages on silicon. The latchup occurs mainly in IO if their design does not take into account the phenomenon, but can also occur in other areas as far as an external stress can reach them. A simple structure of an output buffer is depicted in Figure 7 to explain the phenomenon.

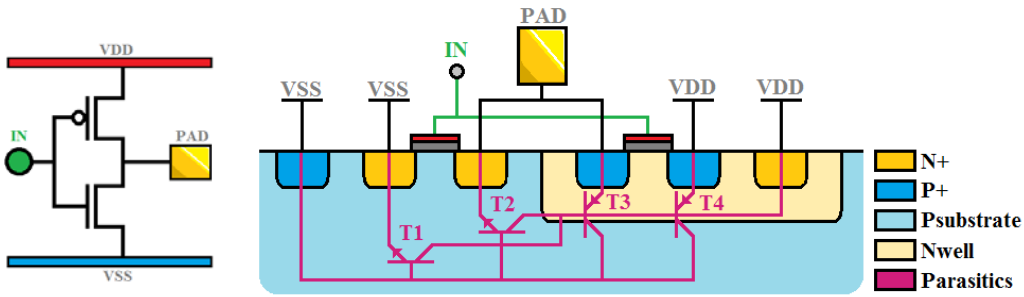


Figure 7: Output buffer schematic and silicon structure with parasitic bipolar transistors

The cross section allows to visualize parasitic bipolar transistors which take part in the latchup phenomenon. An example of a problematic structure built with those transistors is represented in Figure 8.

Regarding the bipolar structure in Figure 8, if the PAD voltage increases over VDD about a diode threshold the transistor T3 turns on. The current from T3 flows in T1 and so T1 turns on and sinks current from transistor T4 which turns on also. The T4 and T1 structure is a low impedance path from VDD to VSS which is hold.

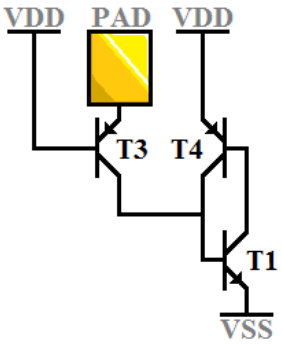


Figure 8: Parasitic problematic bipolar structure

The same kind of phenomenon happens when the PAD goes under VSS with (T2, T4 and T1). More complex conditions can also cause latchup with other parasitic structures or dynamic effects.

2.1.3.1 Latchup test description

The latchup test permits to verify if most common latchup cases are present in the product. It consists in a current sink and injection on each pin and a verification of current consumption on the supply after. If there is no overconsumption on supply, the pin is considered as good. The Table 2 is the test matrix of the latchup test including overvoltage on supply.

Table 2: Latchup test matrix

PIN	Logic state of all IO	Test signal
IO	low	Current sink 100mA
IO	low	Current sink -100mA
IO	high	Current sink 100mA
IO	high	Current sink -100mA
Supply	low	Overvoltage test
Supply	high	Overvoltage test

2.1.3.2 Latchup protection

The first latchup protection is the layout implementation which takes into account parasitic structures. Decreasing bipolar transistor gain by taking collector away from emitter permits to decrease the loop gain of the NPNP structure. Lower the bulk resistance responsible from potential difference when current pass through it help to increase the trigger current. Adding guard ring degrades bipolar transistors gain and diverts current.

2.2 Electromagnetic compatibility (EMC) introduction standards and tests

2.2.1 EMC

The EMC definition is the following one:

"The ability of a device, equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment" [11].

This is a wide definition of EMC, but there are important points to notice. The first one is that EMC concerns device immunity and emission. It means that a circuit can be a victim or an aggressor. The second point is the tolerance notion. Indeed the system has to function "satisfactorily" without introducing "intolerable" electromagnetic disturbances. The difference between a simple dysfunction or a critic dysfunction and a maximum level of emission has to be defined. This is standards job to determine limits. Of course the tolerance level depends also on the application. A dysfunction can be acceptable for a toy whereas it inadmissible for an airplane. Examples are given in Figure 9. Several standards exist depending on the domain (industrial, automotive, medical …).

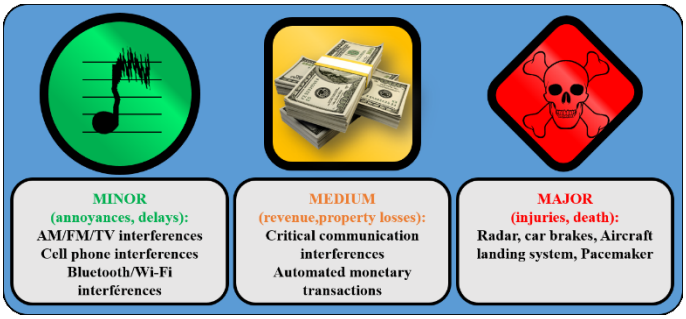


Figure 9: EMC issue gravity

The earliest EMC issues go with first electricity applications in the middle of 18th century [12]. Since this period, EMC understanding hasn't stop to evolve. Nowadays, EMC tend to be an environmental constraint such as

temperature or humidity. At the beginning EMC issues were solved case by case at the end of validation process, but research do not stop to improve models to solve EMC issues earlier in the product life.

2.2.2 EMC management impact on costs

EMC has an impact on reliability of products but also on business and costs. Indeed tests and debug of EMC issues is time consuming and extends the time to market. An EMC issue not fixed in the production step impacts the reputation of the company in term of quality. The Figure 10 compares the EMC cost when considered during the design step and not considered at all. EMC consideration at the beginning increases the costs during the design step. But it lower the number of loop between designers and EMC validations and by this way the pre-production costs. The number of costumer supports decreases also during the production. The loss of customers, going to competitors because of EMC issue, is not represented in the graphic.

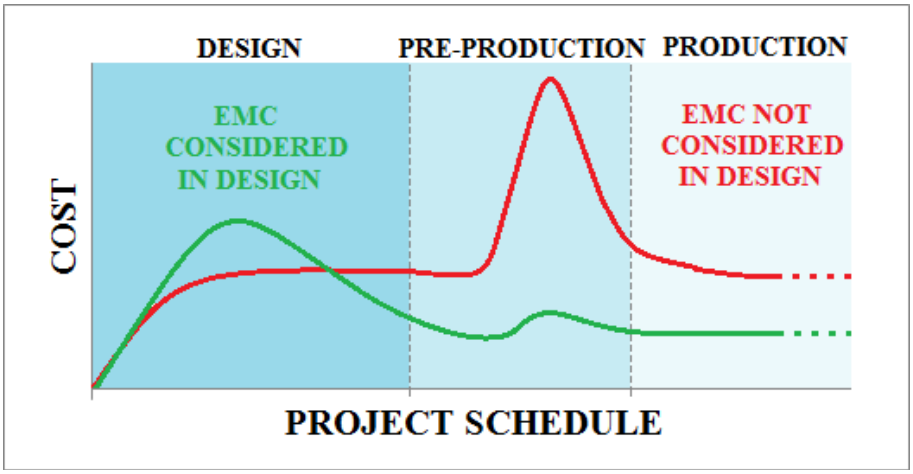


Figure 10: EMC cost comparison

Finding a way to quickly anticipate EMC issues is a serious stake technically and financially. Simulation at the design step would permit to reduce the time to market, customer issue risks and their impact in term of business. Considering EMC at the design step imply to have behavior models for emission and susceptibility.

2.2.3 EMC coupling path and disturbances

2.2.3.1 Coupling paths

Disturbance are transmitted from a device to another by several ways. The Figure 11 illustrates usual coupling path between devices [13]. Notice that each device is a victim and an aggressor at the same time. In the Figure 11, a laptop and a smartphone both connected to supply and their unwanted interactions are represented.

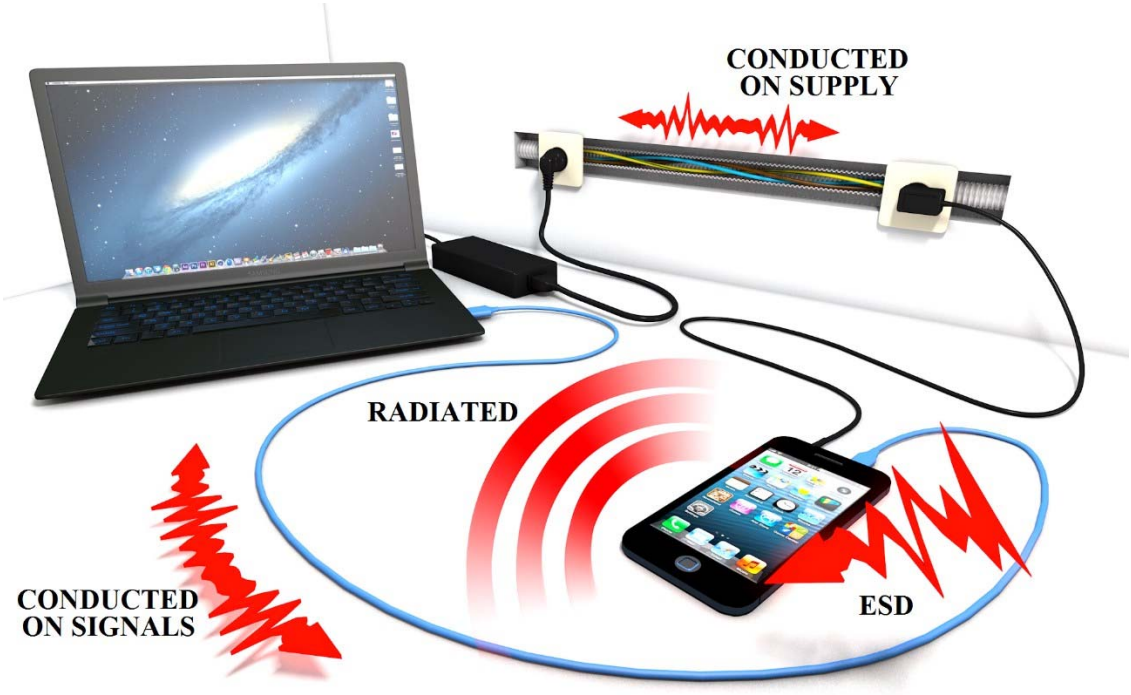


Figure 11: Disturbance propagation modes

The laptop generates a noise which is transmitted to the smartphone by conduction in supply wires. The smartphone activity creates also a perturbation which affects the computer through supply wires. The same phenomenon happens through communication cables. Radiated disturbances are wanted in the smartphone case for communication purpose, but unwanted in the laptop case and due to the device activity, but in all case it induces noise in the environment. ESD has a specific propagation mode, it is conducted but come from external source like a charged human touching the device. It occurs when there is a contact or very close to contact between the source and the device.

2.2.3.2 Disturbances

Unwanted signal can be called disturbance or noise. A noise can be generated by a device or from a natural source. Figure 12 represents a non-exhaustive list of noise sources [14] :

- Natural noise sources
  - Magnetic storm
  - Thunderstorms
  - Atmospheric noise
  - Cosmic noise
- Industrial noise
  - Wireless communication
  - Motors
  - Lights
- Nuclear noise

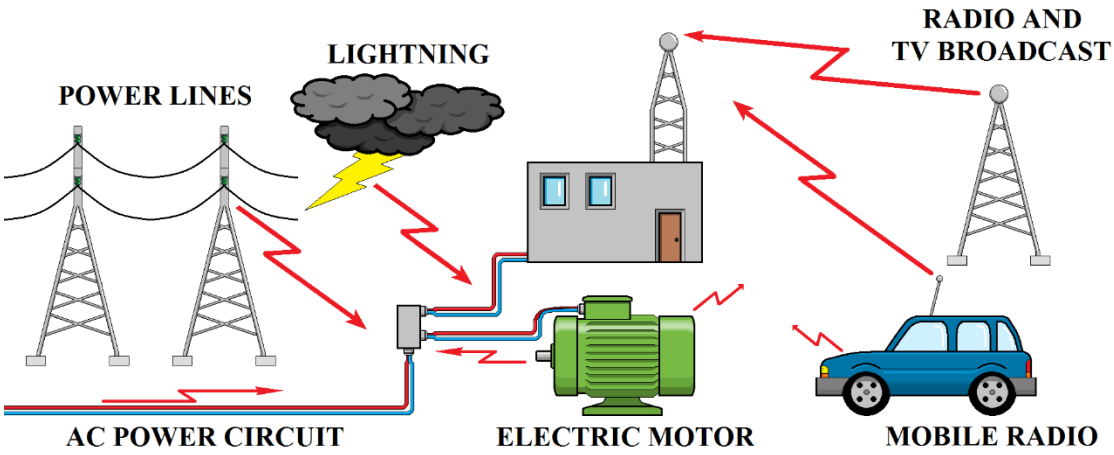


Figure 12: EMC usual noise sources

Disturbance can be classified with their frequency spectrum, their propagation mode and duration. The noise is considered as Low frequency (LF) below 1MHz and High frequency (HF) above. A transient noise has a relatively short duration whereas a continuous noise is steady. This classification permits to have an idea of coupling phenomenon involved in the disturbance propagation.

2.2.4 Standards

Compliance with EMC directives is done by self-certification to harmonized European or international standards. Manufacturer or importer can declare their product conform to a given set of standards, applies the CE mark and markets the product. It is up to the manufacturer to choose the appropriate standard to cover the maximum potential failure, and test it if necessary. The test process can also be done by an external subcontractor.

2.2.4.1 Standard creation flow

Standards propose a way to simulate immunity issues, measure emission of electronic systems, and give harmonized limits and levels. Standards are generated with the organization presented in Figure 13.

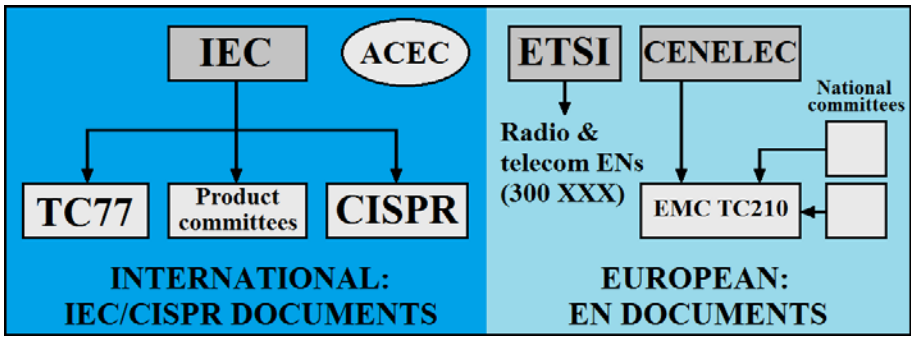


Figure 13: Standards generating bodies

IEC: International Electrotechnical Commission.

CISPR: French acronym for International Special Committee on Radio Interference.

ACEC: Advisory Committee on EMC.

TC77: Is the Technical committee in charge of Electromagnetic compatibility.

ETSI: European Telecommunication Standard Committee.

CENELEC: French acronym for European Committee for Electrotechnical Standardization.

EMC TC210: Technical Committee in charge of EMC activities

TC77 and CISPR are two technical committees from IEC devoted to EMC work for other ones, EMC is only a part of their scope. The ACEC is responsible to prevent the development of conflicting standards in the heart of IEC. European standards are whenever possible based on IEC/CISPR results.

2.2.4.2 Immunity standards

This work is based on IEC immunity standards. Standard are classified with respect to the disturbance type. The IEC standard concerning EMC immunity tests is the IEC 61000 chapter 4 which is divided into several parts. A list of those parts with their description is presented in Table 3 extracted from the IEC website [15].

Table 3: IEC 61000-4-X standard

General
IEC 61000 - Electromagnetic compatibility (EMC) - Part 4-1: Testing and measurement techniques - Overview of immunity tests (IEC 61000-4 series)
LF conducted disturbances
Part 4-11: Voltage dips, short interruptions and voltage variations immunity tests **Part 4-13:** Harmonics and interharmonics including mains signalling at ac power port, low frequency immunity tests **Part 4-14:** Voltage fluctuation immunity test for equipment with input current not exceeding 16 A per phase **Part 4-16:** Test for immunity to conducted, common mode disturbances in the frequency range 0 Hz to 150 kHz **Part 4-17:** Ripple on dc input power port immunity test **Part 4-27:** Unbalance, immunity test for equipment with input current not exceeding 16 A per phase **Part 4-28:** Variation of power frequency, immunity test for equipment with input current not exceeding 16 A per phase **Part 4-29:** Voltage dips, short interruptions and voltage variations on dc input power port immunity test **Part 4-30:** Power quality measurement methods **Part 4-34:** Voltage dips, short interruptions and voltage variations immunity tests for equipment with mains current more than 16 A per phase
LF radiated disturbances
Part 4-8: Power frequency magnetic field immunity test

HF conducted disturbances
Part 4-4: Electrical fast transient/burst immunity test **Part 4-5:** Surge immunity test **Part 4-6:** Immunity to conducted disturbances, induced by radio-frequency fields
Electrostatic discharges
Part 4-2: Electrostatic discharge immunity test

Those standards are made for finished equipment. Microcontroller are not finished equipment but are designed to be a part of such device. EMC immunity and robustness levels are not the same for a microcontroller alone or embedded in a final application. For example, a chip susceptible to ESD stress can be completely safe in a final application if its pins are not accessible by the user. Or on the contrary, good electromagnetic emission with the chip alone can be amplified by the PCB routing of a final application. But in order to give information to customer and help them to make a choice between available products on the market, standards are also used and adapted to chips alones.

2.2.5 Susceptibility EMC tests applied on STM32 microcontrollers

The EMC test flow of a microcontroller includes emission and susceptibility tests. For microcontrollers, two susceptibility tests are performed in our division: Functional ESD (IEC 61000-4-2) and Fast Transient Burst (FTB) (61000-4-4). Only FTB evaluation is studied in this work. However, these two kinds of tests are presented below.

2.2.6 Functional ESD test

The functional ESD test, specified in the 61000-4-2 [3], simulates a discharge when a program is running on the chip. The principle is almost the same as HBM test but the chip is supplied and capacitor and resistor values of the stress generator are not the same. The stress is applied on each pin of the device under test and its behavior is observed. The device has different kind of behaviors. It can function normally when a stress is applied, it can fail and reset,

or it can fail and stay in indeterminate state. Each behavior has its level of gravity and can be acceptable or not depending on the application targeted.

A schematic of the test bench is depicted in Figure 14. This configuration is provided by the standard. Each element has its importance since it can impact the stress shape and thus the behavior of the tested device.

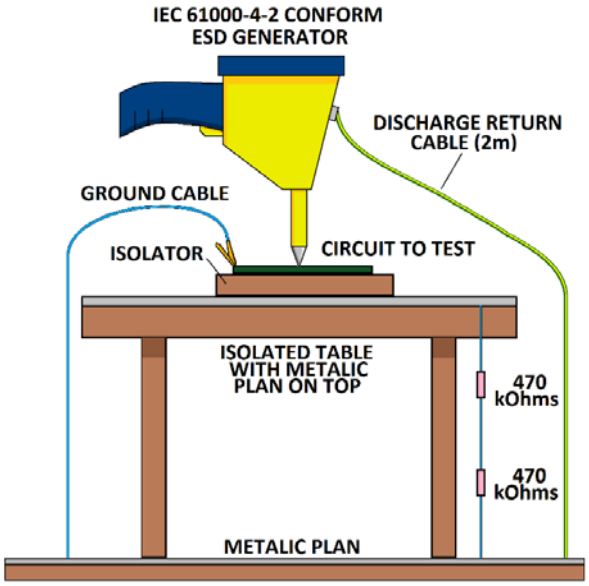


Figure 14: Functional ESD test bench

The test is performed for several voltage levels which go from 200V to 2kV on microcontrollers. The stress generator and stress shape in 50Ω load are described in Figure 15. The stress shape depends on load in which the discharge is applied. The standard describes a specific 50Ω load for the generator calibration.

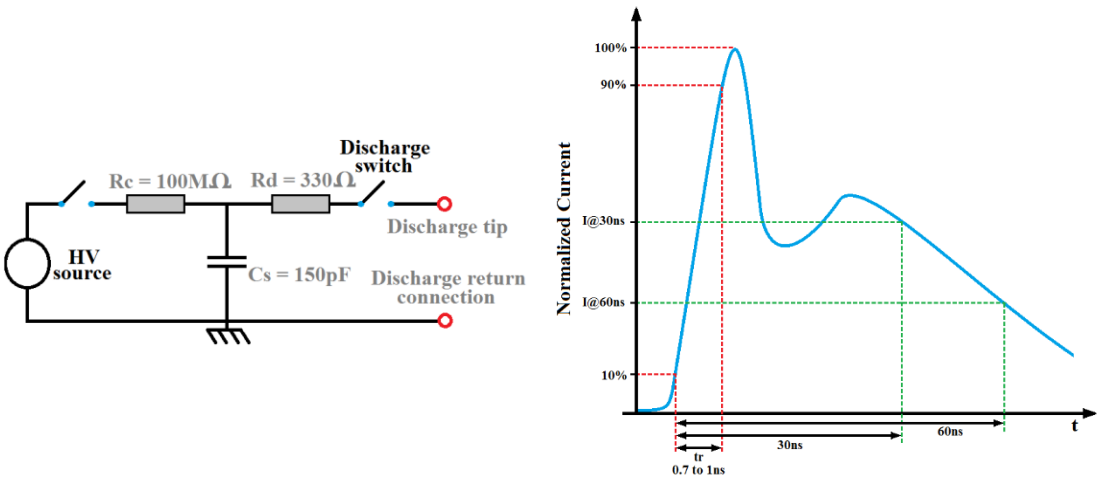


Figure 15: ESD generator principle schematic and stress shape in 50Ω load

2.2.6.1 Functional ESD protection

Even if they are not designed specifically for this stress shape, ESD clamp protections have still an effect when the device is supplied and contribute to its protection. By this way devices are most of time not physically deteriorated. But some latchup effect can still be observed because new coupling paths appear which are not present in the latchup test since the stress shape is more aggressive.

2.2.7 The Fast Transient Burst test

The Fast Transient Burst (FTB) simulates a common mode conducted disturbance. This kind of perturbation happens when several devices have supply or signal wires in the same sheath (illustrated in Figure 16). In this case, if a motor starts, inrush current occurs in its supply cables and creates fast transient voltage variations. Due to capacitive coupling, a disturbance appears on other wires. This noise appears in all cables, this is a common mode perturbation.

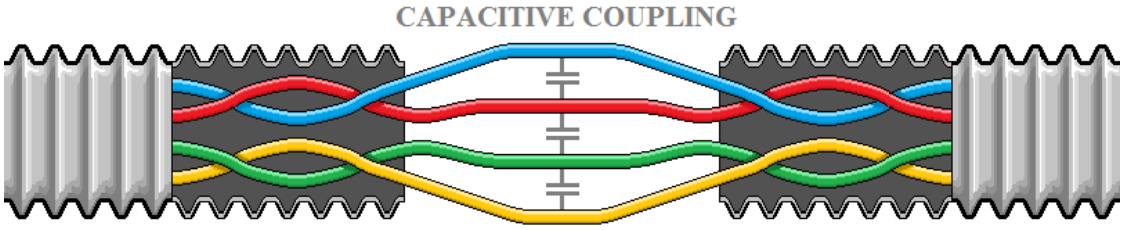


Figure 16: Several cables in the same sheath

The FTB test was developed to take into account the maximum of switching transient cases even repetitive ones at a relatively high frequency (relay contact bounce). The principle of the test is to apply multiple fast transient burst in common mode by capacitive coupling. The FTB stress generator must guarantee specific rise and fall time, and sufficient amplitude. The device under test is supplied by a DC generator and is running. The robustness threshold of the device corresponds to the maximum stress voltage without fail.

2.2.7.1 Test bench description

This work, focuses on a specific FTB test, which is inspired from the IEC 61000-4-4 standard [4] but applied only on supply of microcontrollers. This

standard is normally made for finished equipment, but is used here because there is no other standard which covers those potential fail cases. New standard [16] has been recently published to potentially cover those fail cases but not applied yet. The FTB test bench is presented in Figure 17.

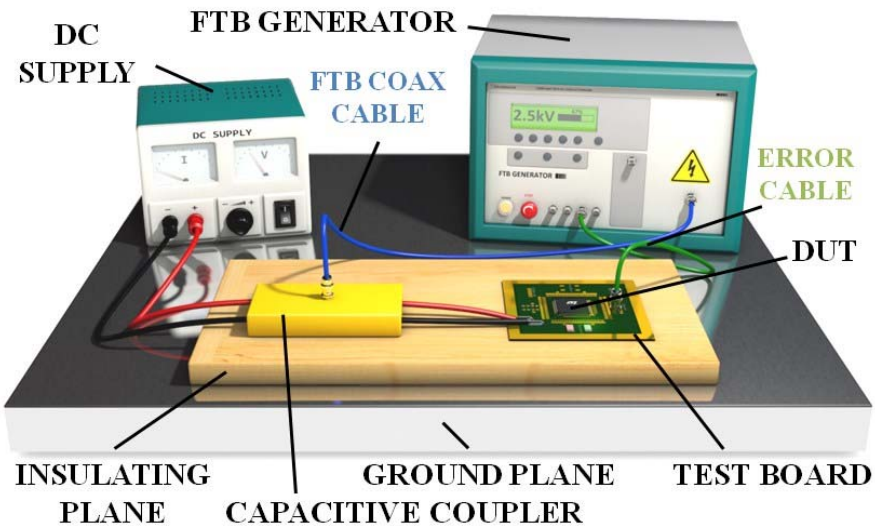
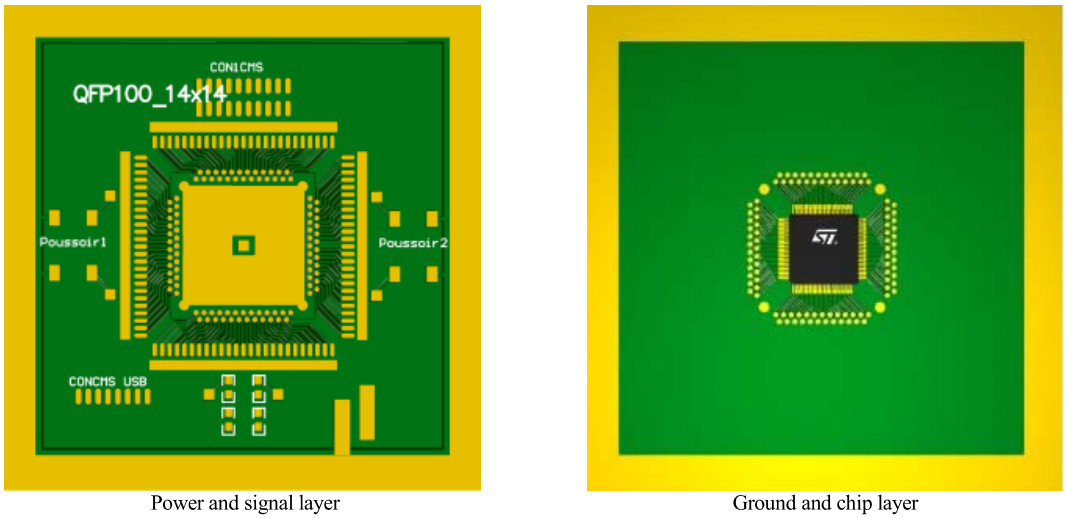


Figure 17: FTB test bench global schematic

During the test, the device under test (DUT) welded on a test board is supplied by a DC Voltage source and the FTB stress is applied on the power supply through a capacitive coupler. The stress is provided by a FTB generator compliant with the standard. In this work, the Schaffner NSG 2025 will be used as a generator. An error return cable transmits the failure information to the FTB generator.

The Test board corresponds to IEC 61967-2 standard [17] with only 2 layers, a ground side and a power and signal side, as shown in Figure 18. Each supply is decoupled with 100nF capacitor as close as possible to the pin. The DUT is in its package and welded on the ground layer side of the test board.



Power and signal layer

Ground and chip layer

Figure 18: QFP100 Test board

A simplified electrical equivalent circuit is proposed in Figure 19. Inductors L_p protect the DC supply from the stress, Capacitors C_c represent the capacitive coupler, and Cc2 is a capacitor which forces a common mode variation. Nets VDD* and VSS* correspond to the local supply after the capacitive coupler. At this point there is a common mode variation with respect to the ground.

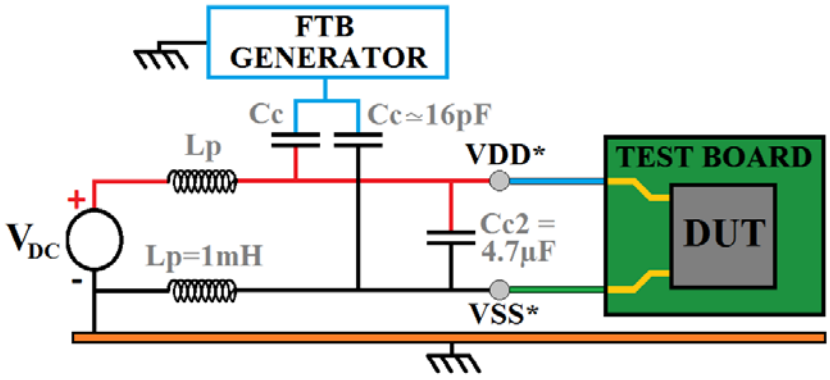


Figure 19: FTB test bench equivalent circuit schematic

For this work the same generic test board will be used with several package footprints. It is also used for each EMC test flow (ESD, FTB, EMI …) and needs to be compatible with all those test benches. A QFP100 version of the board is represented in Figure 18.

2.2.7.2 Test process

A specific test protocol, illustrated in Figure 20, was determined in order to minimize hazards [18]. The first step is done at positive low voltage level (200V), five tests are performed at each steps, the stress level increases until the DUT fails 5 times in a row or the maximum test limit is reached. Once the positive robustness level reached, the stress voltage level is decreased step by step in order to observe an eventual hysteresis phenomenon. The same process is done for negative stress voltages.

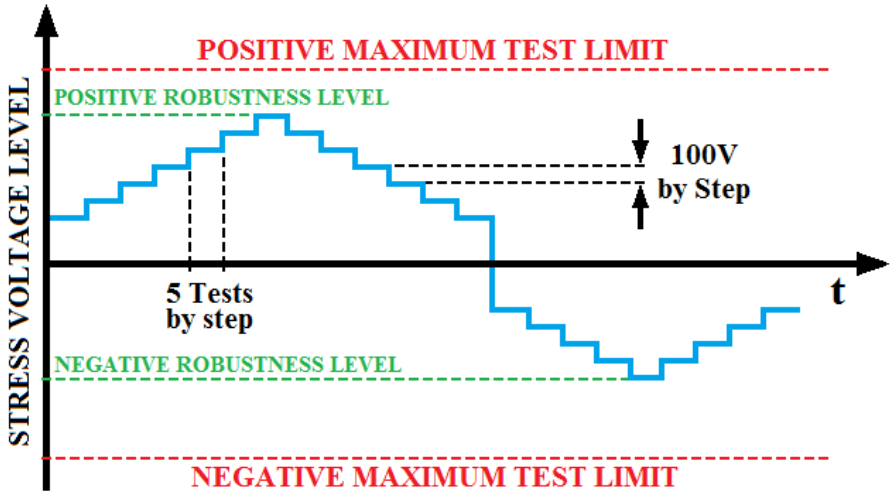


Figure 20: Test process description

The stress shape is described in Figure 21 which is extracted from the IEC standard. For each test the run duration is 12s. Bursts are applied on supply through the capacitive coupler with a repetition period of 300ms. Each 15ms long burst contains 75 pulses.

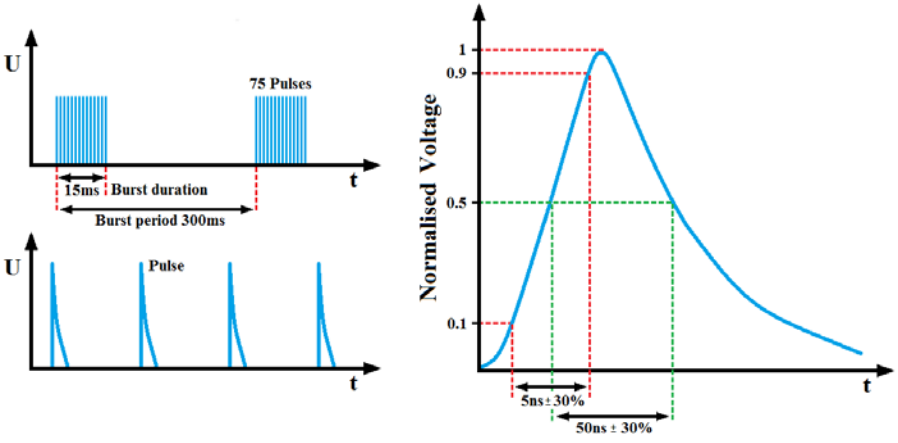


Figure 21: FTB stress shape

The Figure 22 extracted from the standard IEC 61000-4-4 illustrates the stress generator principle. It must guarantee for a unique pulse 5ns rise time ±30% and 50ns fall time ±30%. The fall time is fixed by the size of the capacitor C_c and the resistor R_s. With the given schematic the management of the rise time is left to the implementation of the generator made by the manufacturer of the device.

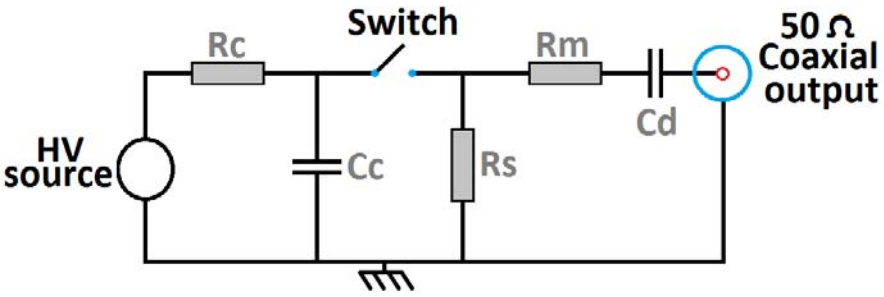


Figure 22: FTB generator equivalent circuit

- R_c = charging resistor
- C_c = energy storage capacitor
- R_s = impulse duration shaping resistor
- R_m = impedance matching resistor
- C_d = DC blocking capacitor

2.2.7.3 FTB protection

There is no specific protection against FTB stress inside microcontrollers. The board implementation integrates decoupling capacitance and so on to decrease noise on supply but they are not placed for FTB purpose and there is no guarantee of their positive effect. The FTB stress mechanism is worth to be studied to find effective protections to improve microcontroller's robustness.

2.2.7.4 FTB analysis state of the art

The FTB test is used to evaluate product robustness. However, the source of bad results at this test is hard to understand. In practice, when a device fails abnormally on a susceptibility test the root cause needs to be found for design correction. Usually, investigations start from the simple information of fail/pass to measurement and eventually simulations. Unfortunately during an

Electrical Fast Transient (EFT) pulse as functional ESD or FTB stress, no measurement is possible due to electromagnetic disturbance (cf. Figure 23). Indeed, coupling on probe cable disturbs measurements when performed during the stress [19]. To provide some answers, the state of the art of the FTB analysis and investigation will be provided in this paragraph.

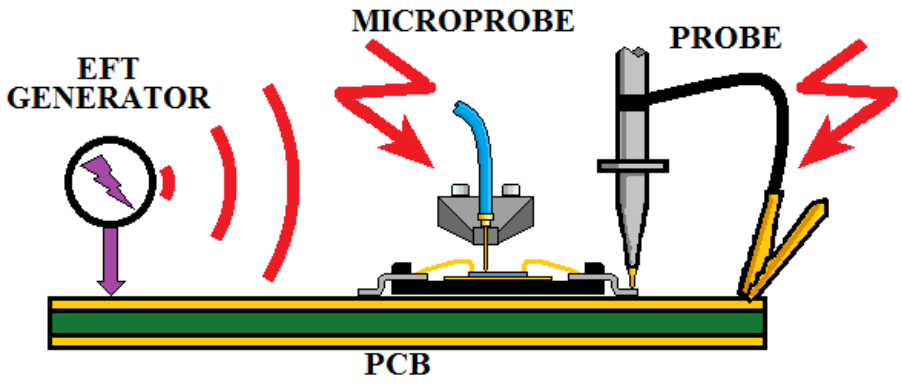


Figure 23: EFT disturbs measurement

Nowadays there is no efficient mean to investigate on FTB test fail other than empiric. Indeed when a fail is detected on a product, the impacted design is protected blindly expecting that the bug will be corrected. This method requires loops between design and validation which are time and cost consuming.

It was seen that no measurement are possible during the FTB stress. What about simulations? Because the stress is in common mode on supply, IBIS models (IO Buffer Information Specification) and IMIC (IO Model For integrated Circuits) are not adapted to the simulation of the stress. Few works deal with the EFT modeling in order to anticipate fails [20] using classic Passive Distribution Network (PDN) model or more complex ones [21].

The ICIM (Integrated Circuit Immunity Model) method is standardized in IEC 62433-4 standard [22] for susceptibility purpose. A principle schematic is depicted in Figure 24.

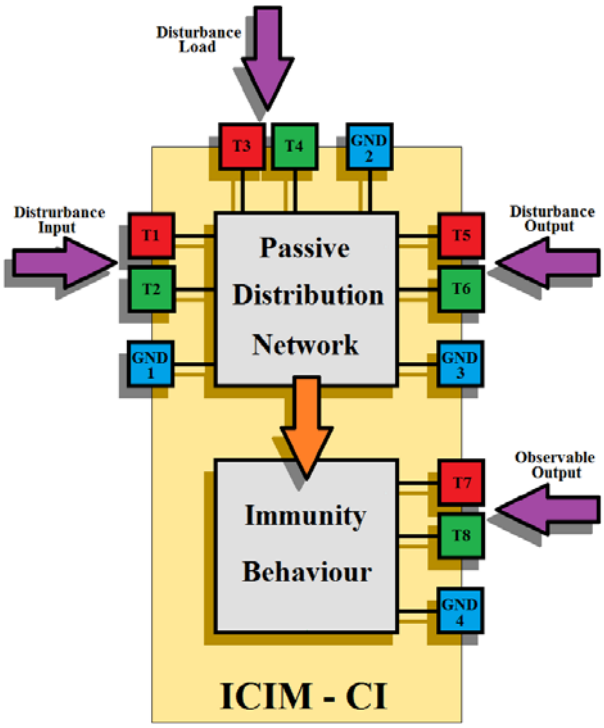


Figure 24: ICIM-CI schematic extracted from IEC 62433-4 standard [22]

This model is composed by a Passive Distribution Network (PDN) and an active part modelled by an Immunity Behavior (IB). The Passive part represents the disturbance coupling path. The disturbance can be introduced through differential input terminals or single ended depending on the modelling level. The Immunity behavior part models the behavior of the device related to the level of disturbance applied. Based on immunity criteria it determines condition for which disturbance causes a fail. No electrical connection is made between the passive distribution network and the immunity behavior model.

The ICIM seems to be the most adapted to simulate circuit submitted to FTB stress. But this approach can't be performed without knowing the injected stress. Indeed it will be seen later in this document that although the disturbance is about thousand volts, the resulting stress inside the die is suspected to be totally different. Without knowing this stress how is it possible to perform simulations?

Knowing stress mechanism is essential to perform efficient simulation and potentially use existing models. By this way it is possible in the end to

predict the test result at the design step. But in a first time, this thesis will try to give keys to understand the FTB stress propagation. It will try to define the resulting stress inside the die and understand fail mechanisms.

3 Conclusion

Microcontrollers are polyvalent system on chip. To meet constraint of all potential applications, they need to be electrically tested for physical robustness and EMC. Among the two EMC test applied on microcontrollers in ST, this work will focus on the particular FTB EMC test.

The FTB test is an EFT in common mode on supply. There is not much publication dealing with this standard concerning ICs. Publication available are about the bench modelling [23][24]. To complete the state of the art, the next chapter is dedicated to the stress propagation mechanism understanding based on the IEC 61000-4-4 standard particularities. Once main mechanism understood, investigation tools will be provided in the Chapter 3 helping to understand fail root causes. This methods and mechanism understandings will be used to improve microcontroller robustness in the last chapter.

Chapter 2 Stress propagation mechanism understanding

Microcontrollers are system on chip designed for a very wide application spectrum. Among electrical tests performed on microcontrollers to guarantee their robustness, this work will focus on the specific EMC FTB test. It consists in applying a common mode stress on supplies while the microcontroller is executing a representative program.

Because the FTB stress is applied on supplies, a first hypothesis is that the quality of the supply network influences the FTB test results. A good way to verify this hypothesis is to test a product with different supply configurations.

Usually for supply integrity purpose, designers ask for the maximum supply couples as possible. It decreases the resistance and inductance effect of supply nets and improves the power quality. It is also better for electromagnetic emission as current in each supply loop is lower when it is distributed around the chip. To reduce electromagnetic emission, ground wire needs to be as close as possible to power wire to decrease loops size.

For marketing purpose the less supply couples there are, the more functionalities can be sold to a customer for a same package. So a compromise needs to be done between power integrity, emission, and available functionalities to optimize the supply pin number.

1 Supply pin number and placement consequence on FTB test results

Microcontrollers allow different supply setup for a same chip. A good way to know if only the chip is responsible of the robustness threshold or if the external supply network influence the FTB test results is to test the same chip with several bonding configurations.

Tests are performed on STM32FXX product in TQFP100 package. Using different bonding diagrams allows to change the number of supply around the same die. It is possible to change the number of VDD or VSS independently as well as the number of external regulator capacitor (Vcap).

Several bonding diagram setups, from the minimum supply number to have a functional chip, to the maximum supply pads connected, were tested. Between the two extremes, illustrated in Figure 25, several variations are named with the following method: Number of VDD Number of VSS Number of VCAP (external regulator capacitor). For example, 221 (the minimum supplies number, cf. Figure 25) means 2 VDD, 2 VSS and 1 VCAP connected.

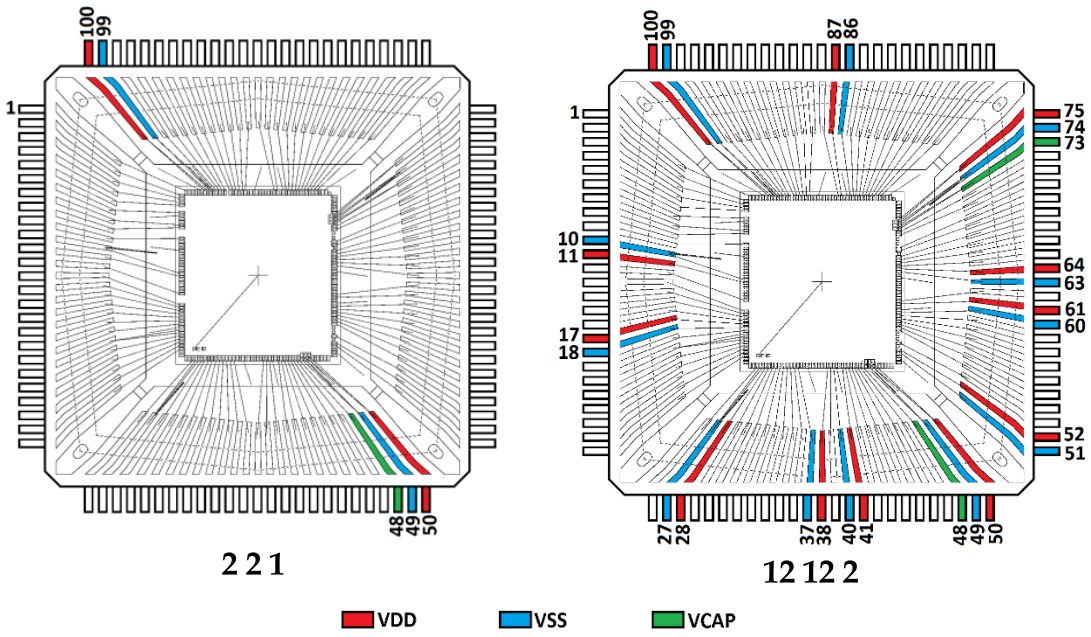


Figure 25: The minimum and the maximum bonded supplies

1.1 Results

1.1.1 The impact of external regulator capacitor number

The measured chip has an internal regulator which needs external capacitors. There are two available pads to connect external capacitors named Vcap. To study the impact of Vcap number on the FTB robustness, several bonding with one or two Vcap were tested. Results are presented in the Table 4.

Table 4: Vcap influence on FTB test results

Nb VDD	Nb VSS	Nb Vcap	FTB_{th+}	FTB_{th-}
5	5	**2**	>3.5kV	<-3.5kV
5	5	**1**	>3.5kV	<-3.5kV
4	4	**2**	3.0kV	-2.9kV
4	4	**1**	2.6kV	-2.5kV

Chips with bonding diagram 551 and 552 have robustness threshold up to the maximum test voltage. However, the 441 and 442 configurations permit to conclude that the number of external regulator capacitor affects the FTB test results. For all the next bonding configurations two Vcap will be kept.

1.1.2 The impact of the number of supply couples

The number of supply couples is often challenged by marketing teams. Indeed in a given package the more supply pin there are, the less functional IOs are available. Decreasing the number of supply permits to sell more functionalities but affect microcontroller's performance and robustness. This test will permits to know how the robustness is impacted.

The influence of supply couples amount on the robustness results is measured by testing bonding diagram with the number of VDD equals to the number of VSS. Notice that supply couples are smartly placed around the chip (VDD wire is next to the GND wire and uniformly distributed) and no singular bonding diagram is tested with respect to usual rules. FTB test results are graphically represented in Figure 26.

With such results, it seems that the more supply couples there are, the more robust the microcontroller is. But to validate this hypothesis several placements for a given number of supplies will be tested.

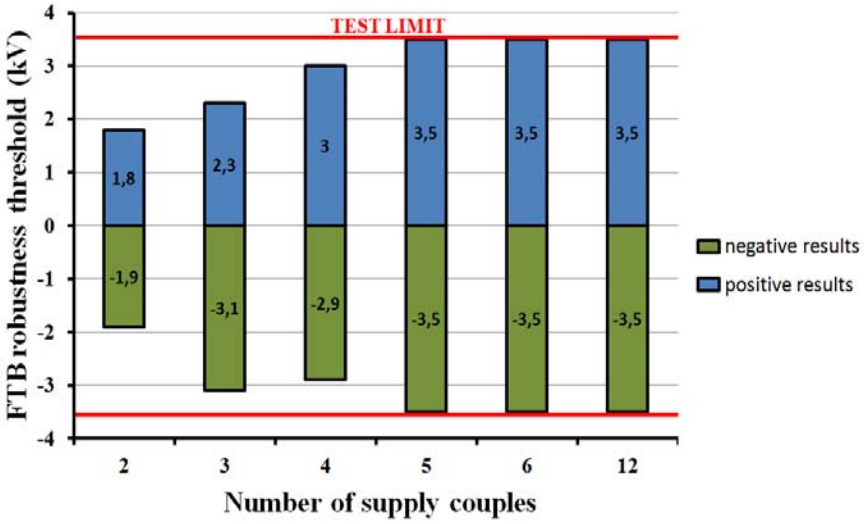


Figure 26: Graphical representation of number of supply couples influence

1.1.3 The impact of the supply placement

As there are 12 available supply pads on the chip, it is possible for low count supply couples, to change their placement. Bonding diagrams with the same number of supply couples are measured. The 442 configuration is chosen because its results on the previous test are under the maximum test limit. By this way, improvement or degradation would be observable. For supply placements described in Figure 27, singular placement like separated VDD and VSS (442 version 4) or non-distributed supply around the chip (442 version 3) are evaluated. Notice that the previous 442 bonding diagram corresponds to the version 1.

FTB test results are summarized in Table 5. The previous hypothesis regarding the number of supply requires a deeper analysis. Indeed, the supply placement has also a significant influence on the FTB robustness voltage threshold. It can change results positively or negatively.

Table 5: Supply placement influence test results

Bonding	version	FTB_{th+}	FTB_{th-}
442	**1**	3.0kV	-2.9kV
442	**2**	>3.5kV	<-3.5kV
442	**3**	2.2kV	-1.3kV
442	**4**	2.1kV	-1.6kV

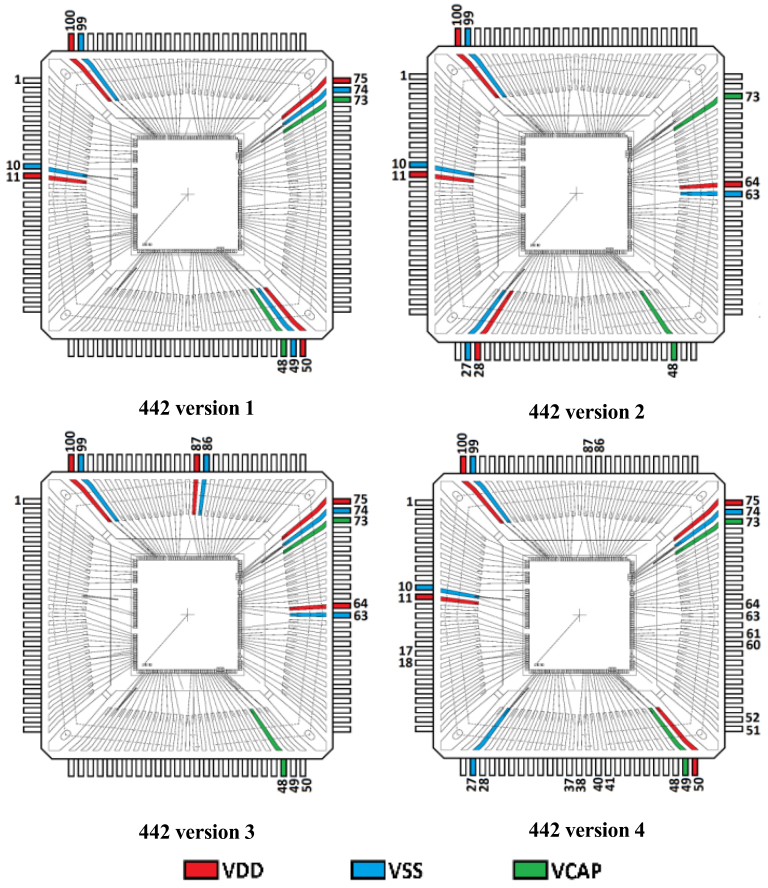


Figure 27: Supply placement influence

1.2 Conclusion about results

The number of external capacitors, the number of supplies and the placement of those supplies are able to change the robustness threshold in a wide amplitude. Results provided by this study permit to affirm that the chip is not the only contributor to the FTB test robustness. The supply network and the bonding diagram in particular has a sensible effect on the robustness to FTB stress.

No clear rules can be extracted from this study. But classic design rules, such as mores supply pair as possible, GND close to VDD, supply distributed around the chip, are not enough to protect a chip from the FTB stress.

Beside those results which show that bonding diagrams impact the susceptibility, there is no reason that the PCB escapes to this rule. It is clear that

the supply network, including PCB, bonding wires and silicon, influence the stress propagation and its effect on the microcontroller behavior.

How does the stress go through this network from the injection point and disturbs circuits inside the die? Seeing results presented before, the hypothesis that fails are caused by the common mode to differential mode conversion seems to be the most obvious. This hypothesis will be explained in the next section.

2 Common mode to Differential mode conversion hypothesis

This section is dedicated to the understanding of the common mode disturbance and its implication in the circuit disturbance. The mechanism which transforms the common mode stress into a differential stress will also be broached.

2.1 Common mode on supply

The particularity of the FTB stress is that it is a common mode disturbance. If it is applied on a device supply, the reference node (GND) and the power node (VDD) vary at the same time with the same amplitude with respect to the ground. It means that the device supplied between those two nodes sees the same voltage VDD – GND during all the common mode variation as shown in Figure 28.

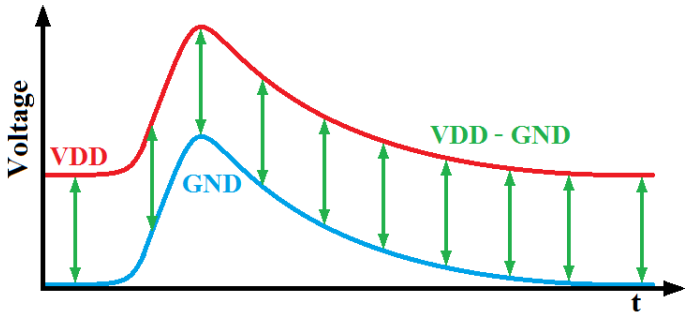


Figure 28: Common mode variation

A priori an electric device can't be disturbed by a common mode disturbance on its supply if nodes impacted are its only references. This is the case of microcontrollers when only one supply is used. But this is not what is observed during a FTB test as the microcontroller fails anyway. This observed behavior leads to the following question.

How a common mode perturbation on supply can disturb an electronic device? A common mode stress can be transformed into a differential mode stress in certain conditions. This conversion will be explained in the following section.

2.2 Common mode to differential mode conversion understanding

A common mode variation on supply cannot disturb an electrical circuit, only differential mode disturbance can impact its behavior. The hypothesis which follows from that, is this one:

The common mode stress is converted into a differential mode between the injection point and inside the die.

It is of course not possible if the supply network is considered as two perfect wires for the power and the ground. What if we consider imperfect wires for power and ground? To understand what happens, a simple model is proposed representing two supply wires. This model given in Figure 29 takes into account the resistance, the inductance and the capacitance of wires with respect to ground.

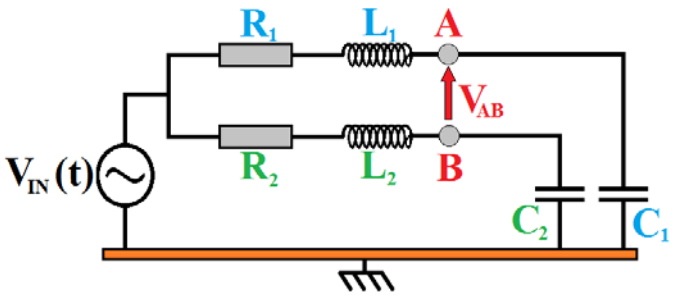


Figure 29: Simple supply wires model

The signal V_{IN} represents a common mode disturbance, the capacitive coupler is not represented, and this is a AC simplified schematic. If R1 = R2, L1 = L2 and C1 = C2, voltages on A and B with respect to the ground are the same. V_{AB} is constant, an IP supplied between A and B would see the same voltage.

If just one of R, L or C parameter is modified, voltages at A and B points are not the same anymore, V_{AB} is not constant. By introducing a common mode stress a differential variation appears. The Figure 30 show a simulation with only a difference on wires inductance. The first wire has an inductance of 20nH which correspond approximatively to a 2 cm length and the second 25 nH for a 2.5 cm length wire. The input signal V_{IN} is a simple step.

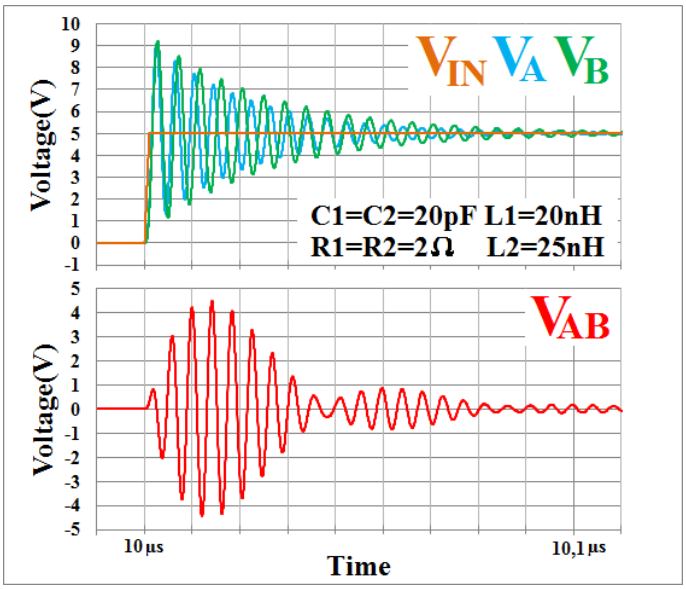


Figure 30: Common mode into differential mode conversion

It is possible to make the same model with the order of magnitude of bonding wire in a QFP package. The inductance value is around 2nH for a QFP100 bonding wire and resistance approximately equal to 100mΩ. The capacitance of the VDD and VSS nodes with respect to the ground if the insulating plane of the FTB test bench is 10cm thick is around 10fF depending on the size of the chip (cf. Figure 17, page 20). In a QFP package the wire bonding length varies by 40% depending on their placement. In Figure 31 the differential voltage is plotted for L1 = 2nH and L2=2.5nH, which correspond to 0.5mm length difference, and a single stress amplitude of 1kV.

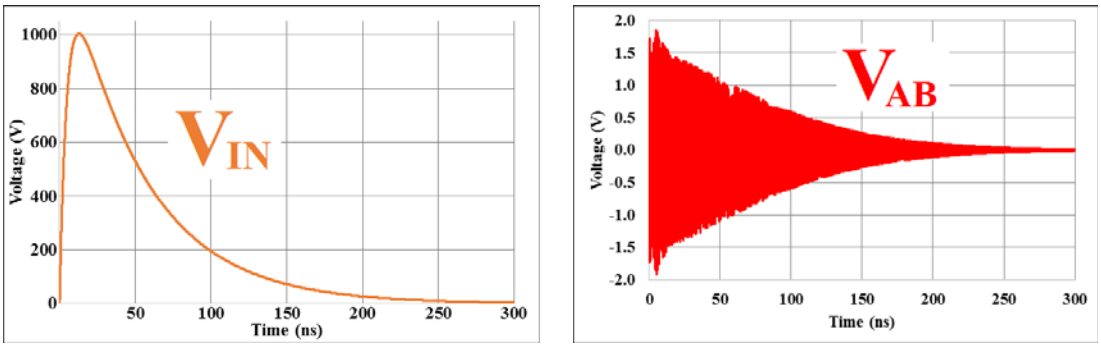


Figure 31: Common mode to differential mode conversion QFP order of magnitude

By modifying the bonding diagram, the way by which the common mode is converted into the differential mode changes. So the stress seen by internal IPs changes for each kind of bonding too. As it is a mismatch issue we can suppose that increasing the number of supply bonding wires only contributes, to average and therefor lowering the difference between paths.

Indeed, if the same kind of model is made with multi supply bonding wires instead of simple supply couple, it would give the circuit in Figure 32. To simplify it, only bonding wires are represented, but to be more accurate, the printed circuit board and the supply network on the silicon might be also modeled.

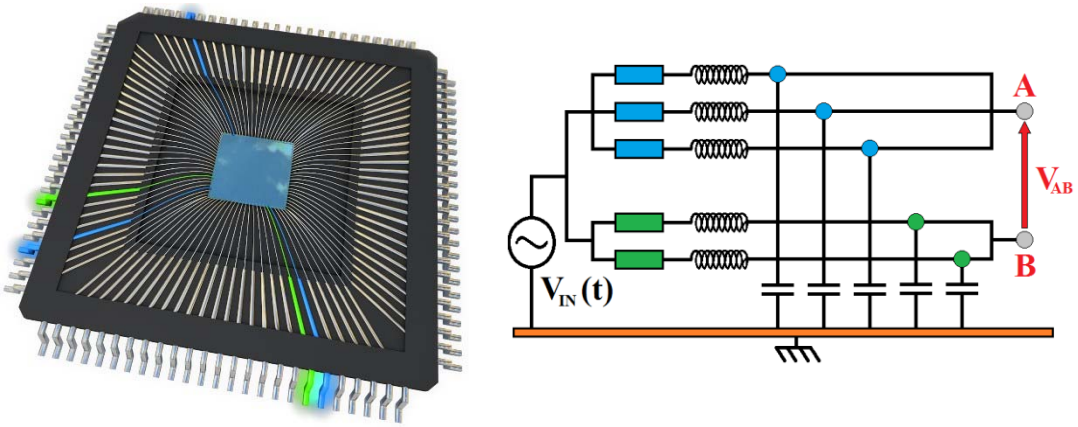


Figure 32: Simplified multi supply wire bonding model

There are still two paths from the signal generator to a point A and another to point B. But the number of influent parameters on common mode to differential mode conversion is much higher than with only two wires. Those

parameters depend on bonding wires length, wires height with respect to the ground plane, their geometry, and their material. It is almost impossible to have the same path from the signal generator to point A and B because of several reasons such as mechanic constraints for connections which induce tolerances, imperfections on materials and so on.

For the FTB test, all paths between the stress injection point and the supply points of a weak intern circuit have to be taken in account to understand a failure.

2.3 From concept to reality

A way to convert a common mode stress into a differential mode stress is identified. But imperfections of supply network such as capacitance or inductance have an impact which depends on frequency. The sensitive frequency range depends on the order of magnitude of those parasitic elements and so on the implementation of the supply network in the test conditions.

The next section is dedicated to the study of influencing parasitic elements of the supply network. It will lead to conclude if they are significant enough to provide a differential stress able to disturb circuits inside the chip in real conditions, and for which frequency range.

3 Main parameters on common mode to differential mode conversion

A key factor on FTB test failure understanding is the common mode to differential mode conversion of the disturbance. The encountered phenomenon has been described in the previous part. The common mode to differential mode is caused by the difference between the VSS and VDD path from the stress injection point to the tested circuit. In a first time, the microcontroller is considered as the tested circuit. But a microcontroller is by itself a complex assembly of several circuits, so it is possible to consider one of those circuits as

the test target. By this way the internal parameters of the chip have also their contribution.

Influencing parameters will be studied from the bigger in terms of size to the smaller as illustrated in Figure 33.

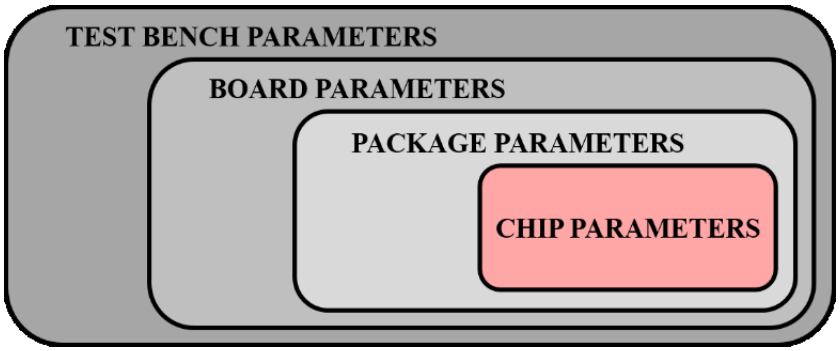


Figure 33: Influencing parameters studying parts

Each part has its specificities and interacts with each other. No precise value will be given, but only the order of magnitude. Indeed parts of the test bench are handmade and subject to mechanical tolerance, and this study is intended to be as general as possible.

3.1 Test bench parameters

In this paragraph, the test bench refers to the stress generator, cables and the capacitive coupler. The test board, the package and the die will be studied in next parts. Formulae to calculate most encountered parasitic elements are also introduced in this section.

A schematic of the entire test bench is given in Figure 17 (page 20) and a simplified electrical equivalent schematic in Figure 19 (page 21). The capacitive coupler is considered as perfect and L_p protection inductors as an open circuit for the stress. However, there are wires between the capacitive coupler and the test board which can be modeled with a RLC circuit as represented in Figure 34.

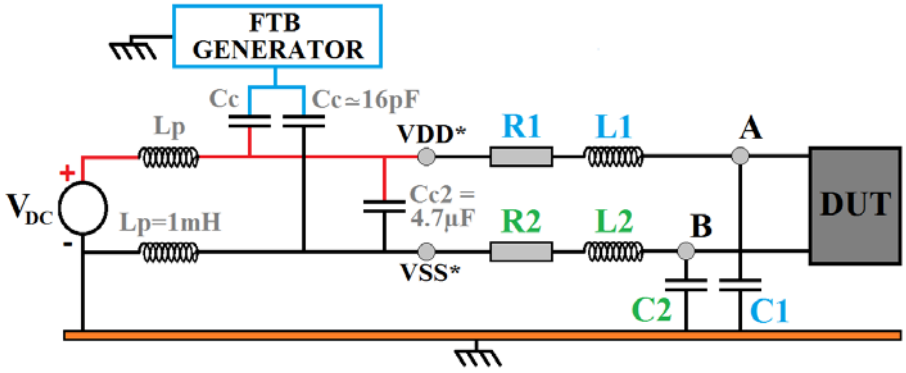


Figure 34: Test bench influencing parameters representation

Connection from the capacitive coupler to the test board is handmade and usually not considered as critical. The tolerance on the length is estimated to 20%.The resistance of wire, illustrated in Figure 35, can be calculated with the following formula:

$$R = \frac{\rho . l}{S}$$

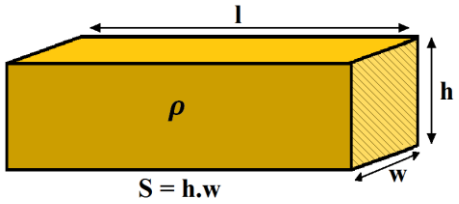


Figure 35: Resistance formula

Where σ is the resistivity of the material, l its length and S the surface of its cross-section.

0.2 mm² and approximately 10cm length copper wires are used. For copper at 20°C, $\sigma = 1.68.10^{-8}\Omega.m$ so the resistance of wires is less than 10mΩ.

Accurate calculation of the inductance of a wire can be very complex. Several formulas exist depending on the geometry of wires and their configuration [25] with respect to the ground or more generally the current return path. A formula for a cylindrical conductor in parallel with a perfect conductor at low frequency is given in Figure 36. To estimate the inductance of a wire it is also possible to use the approximation 1mm ≈ 1nH. Here the inductance of 10cm wire is close to 100nH. Inductance calculator are also available online [26] and give a value of 114nH. Technically the approximation give a value accurate enough and will be often used in this work.

$$L = \frac{\mu_0 . \mu_r}{2\pi} . l . \left(ln\left(\frac{2h}{d}\right) + \frac{1}{4} \right)$$

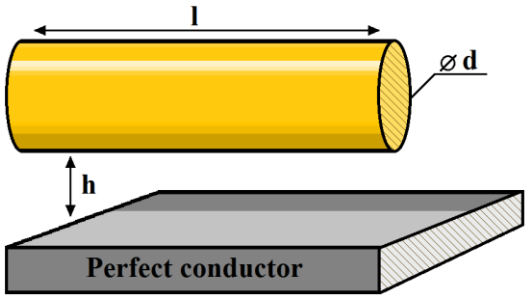


Figure 36: Inductance formula

Where μ_0 is the permeability of the vacuum μ_r the relative permeability of air, l its length of the wire and d its diameter.

Capacitance between VDD net and VSS net with respect to the ground (here represented by C_1 and C_2) has a significant influence on the FTB test results. Indeed this is the only path from the generator to the ground plane. This capacitance is made by all wires, VDD and VSS plane of the board and power network of the chip with respect to the ground plane. The capacitance of wires will not be calculated here because it is negligible compared to the one of the board, but capacitance formula is reminded in Figure 37.

$$C = \frac{\varepsilon_0 \varepsilon_r S}{d}$$

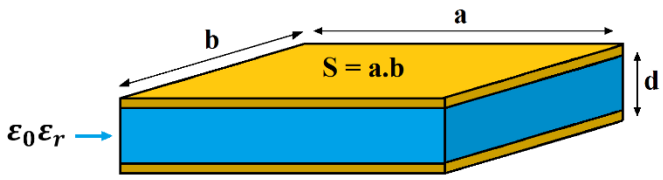


Figure 37: Capacitance formula

Where, ε_0 is the electrical constant ($\varepsilon_0 = 8.854.10^{-12} F.m^{-1}$), ε_r is the relative permittivity of the dielectric, S surface of planes and d the distance between them.

The capacitance depends on the permittivity and the thickness of the insulating plane. A microcontroller was tested with an insulating plane 10cm thick and then with a 3mm thick made of the same material. Results are summarized in Table 6.

Table 6: Insulating plane thickness comparison on a FTB test result

Insulating plane thickness	FTB_{th+}	FTB_{th-}
10 cm	2kV	-2.6kV
3 mm	1.1kV	-1.9kV

All next tests will be done with a 10cm thick insulating plane. There is also a capacitance between VDD and VSS nets but it is also negligible compared to the one of the board and the capacitance C_{c2} (at low frequency).

Main influencing parameters of the test bench are wires between the capacitive coupler and the thickness of the insulating plane. It is important to keep in mind that the difference between the VDD and VSS path causes the common mode to differential mode conversion. Here the tolerance is relatively high on all elements because it is handmade and arbitrary placed on the ground plane. To limit differences, a specific insulating plane depicted in Figure 38 with all elements fixed on it is used.

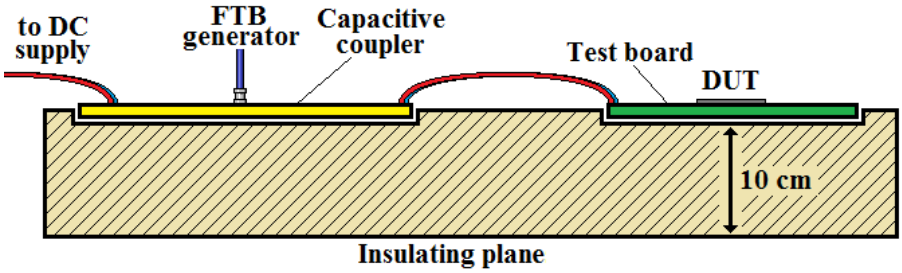


Figure 38: Specific insulating plane schematic

On this insulating plane, a cavity is milled to block the test board in all directions and keep it at a constant distance from the ground plane. The coupling capacitor is also fixed to the insulating plane to keep it at a constant distance from the test board. This precaution insures a reproducible placement of test bench elements.

The Table 7 summarizes the order of magnitude of RLC parameters studied in this part considering VDD path in red, VSS path in blue and

interaction between them in green. This kind of table will be used for each studied parts in this chapter.

Table 7: Test bench RLC summary

PART			Parameter	Approximated value	Comment
TEST BENCH	R		R_{wire_vdd}	<5mΩ	Neglected
			R_{wire_vss}	<5mΩ	Neglected
	L		L_{wire_vdd}	100nH ±20nH	
			L_{wire_Mutual}	25nH ±15nH	Neglected
			L_{wire_vss}	100nH ±20nH	
	C		$C_{wire\_vdd\_gnd}$	<10fF	Neglected
			$C_{wire\_vdd\_vss}$	<10fF	Neglected
			$C_{wire\_vss\_gnd}$	<10fF	Neglected

3.2 Test board parameters

During the test, the DUT is welded on a test Board (represented in Figure 18 page 21). Each DUT supply is decoupled with 0805 100nF SMD capacitor as close as possible to the pin. The DUT is welded on the ground layer side. In the simplified board supply equivalent circuit (cf. Figure 39), the capacitor C_b represents the capacitance between the two supply layers of the test board. C_{c1}, C_{c2}, and C_{cn} correspond to decoupling capacitors. C_{gvss} and C_{gvdd} symbolize respectively the capacitance of the VSS plane and VDD plane with respect to the ground. L_{vdd} and L_{vss} represent the routing from the VDD and VSS plane to the package.

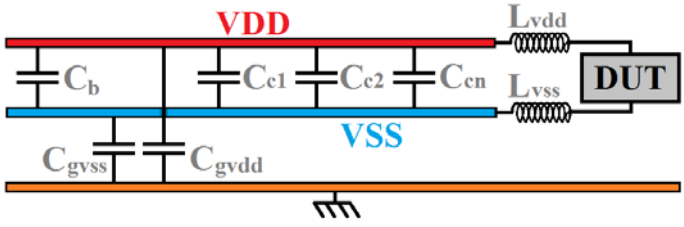


Figure 39: Test board simplified supply equivalent schematic

C_b is made by parallel supply planes, and can be calculated with the dimensions of the board. The ground plane is on almost all the area (10cm by 10cm) and the power plane is smaller because it has to share the surface with

signals wires. The Table 8 gives order of magnitude of the impedance of the board at some frequencies.

$$C_b = \frac{\varepsilon_0 \varepsilon_e \, S_{vdd.gnd}}{d} = \frac{8.85.10^{-12} \,.3.6\,.50.10^{-4}}{1.5.10^{-3}} = \; 106pF$$

Where:

- *d thickness of the test board = 1.5mm*
- *εe is the relative permittivity of the epoxy (which is 3.6)*
- *ε_0 is vacuum permittivity 8.85pF/m*
- *$S_{vdd.gnd}$ is the surface of VDD plan which is smaller than GND plan.*
- *Cc is decoupling capacitors added on test board between VDD and GND too.*

Fringe capacitance and skin effect are neglected

Table 8: Board capacitance impedance order of magnitude

Frequency	**106pF capacitance Impedance $Z_c = \frac{1}{2\pi FC}$**
100MHz	16Ω
200MHz	8Ω
400MHz	4Ω

C_{gvss} and C_{gvdd} are calculated with the same formula but the distance between conductors correspond to the insulating plane thickness (10cm).

$$C_{gvss} = 5pF \;\; C_{gvdd} = 2.5pF$$

Capacitors C_{cn} are 100nF SMD decoupling capacitors which are welded at each DUT supply connection between the supply wire itself and the ground plane. The number of SMD capacitors depends on the DUT number of supplies. Those capacitors are not perfect, they have parasitic serial inductance which limit their effect at high frequency. The Figure 40 shows the impedance variation of a 100nF SMD versus frequency.

Capacitance between VDD and VSS nets tends to limit the common mode to differential mode conversion whereas capacitance with respect to the ground tend to makes nets independent one over the other.

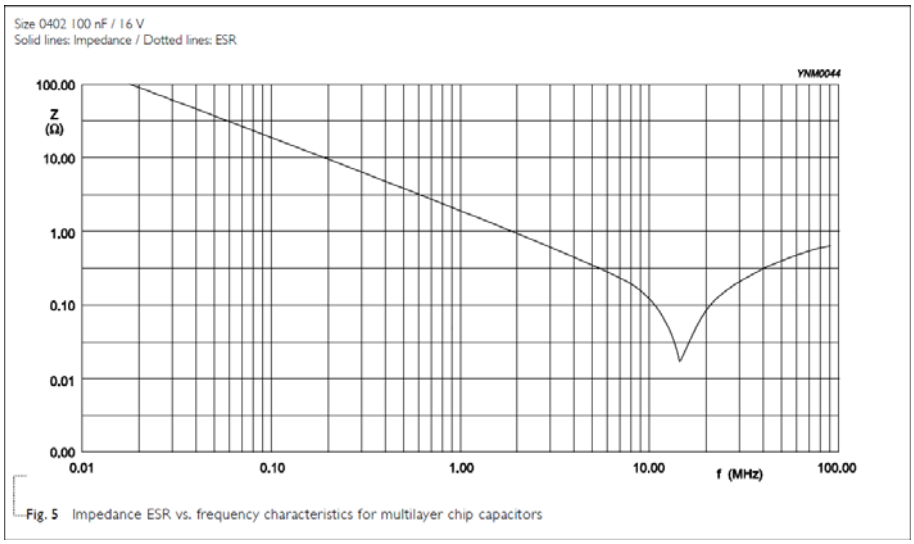


Figure 40: SMD capacitor impedance versus frequency extracted from YAGEO Datasheet [27]

In a usual practical case where the DUT has 4 supply couples, C_b is parallel to four C_{cn}. The equivalent capacitance of the total board between supply planes up to 10MHz is 400nF. By taking into account the efficiency loss of capacitors, at 100MHz, the impedance between supply planes of the board is around 0.25Ω whereas the impedance of VDD and VSS with respect to the ground are respectively 300Ω and 150Ω. VDD and VSS have a huge tendency to vary in common mode around 100MHz before the routing from supply planes to package.

SMD capacitance are welded on the signal side of the board. There are wires (L_{vdd} and L_{vss}) from the decoupling capacitors to supply pin of the DUT package. The Figure 41 represents the routing on ground layer side, for a DUT with four supply couples.

The length of supply routing for a QFP100 test board can vary from 4mm to 7mm. Those lengths can change depending on the test board used but with the same order of magnitude. Actually L_{vdd} and L_{vss} correspond to several separated inductances not represented in Figure 39. This inductive path does not stop to the package pin, but continues inside the package.

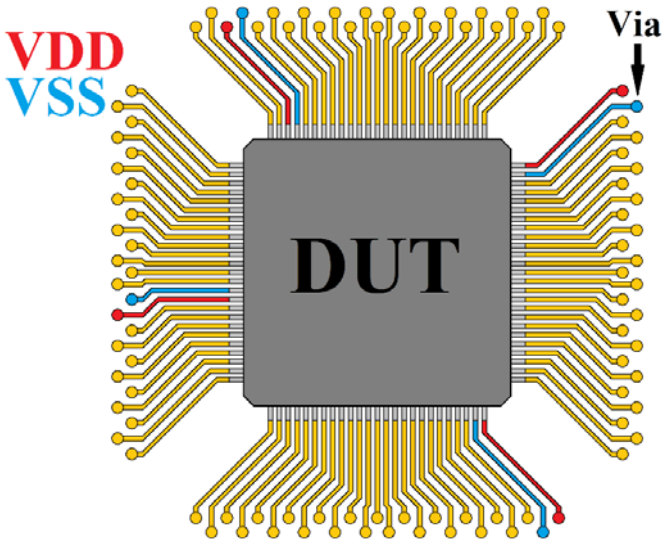


Figure 41: Board parameters schematic

From the stress injection point to those board tracks, VDD and VSS paths are made of the test bench wires mainly inductive and the board planes mainly capacitive. The routing which go to package pin are less inductive than test bench wires but could introduce big differences between VDD and VSS paths. It is also conceivable to don't have the same number of VDD and VSS tracks. This kind of mismatch increases the common mode to differential mode conversion.

The Table 7 summarizes values mentioned during the previous paragraph. Inductance values are given for a single track. The next paragraph deals with the package which is the continuity of routing track studied in this one.

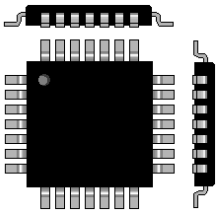
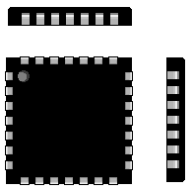
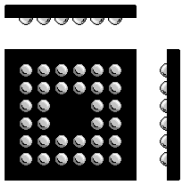
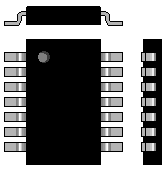
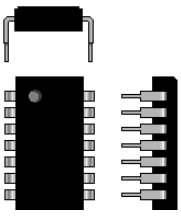
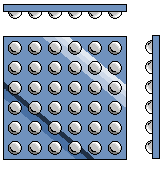
Table 9: Board RLC summary

PART		Parameter	Approximated value	Comment
BOARD	R	R_{board_vdd}	<1mΩ	Neglected
		R_{board_vss}	<1mΩ	Neglected
	L	L_{board_vddn}	6nH ±2nH per track	
		L_{board_Mutual}	Depend on routing	Neglected
		L_{board_vssn}	6nH ±2nH per track	
	C	C_{gvdd}	2.5pF	
		C_b	100pF	
		C_{cn}	100nF per supply pair	SMD capacitor
		C_{gvss}	5pF	

3.3 Package parameters

Microcontrollers are encapsulated in different kinds of packages. The Table 10 provides a non-exhaustive list of usual microcontroller's packages.

Table 10: Microcontroller usual packages

Package Name	Description	Schematic
QFP	Quad Flat Package: surface mounted wire bonded package.	
QFN	Quad Flat No lead: surface mounted, wire bonded, thermal pad to improve heat transfer.	
BGA	Ball Grid Array: surface mounted, wire bounded, Short lead frame, high connection density.	
SOIC	Small Outline Integrated Circuit: surface mounted, wire bounded, for low pin count.	
DIP	Dual Inline Package: through hole mounted, wire bonded, for low pin count.	
CSP	Chip Scale Package: no wire bonding, custom lead frame, the smallest, high connection density.	

Each package has its own specificities but there is always a pin (or a ball) to make the connection to the PCB, and a lead frame and a wire bonding (except for CSP) to connect the pin to the chip pad.

For practical purpose, the QFP package will be used most of times in this document. Indeed this package can be easily hand welded, and allows a relatively high pin count. Its leads frame and bonding wires provide non negligible inductance and makes this package a good study case. The Figure 42 shows how the connections are made inside the package, pins, lead frame and bonding wires are visible.

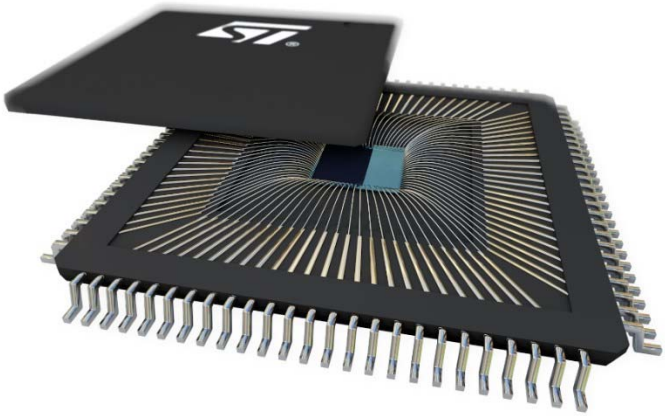
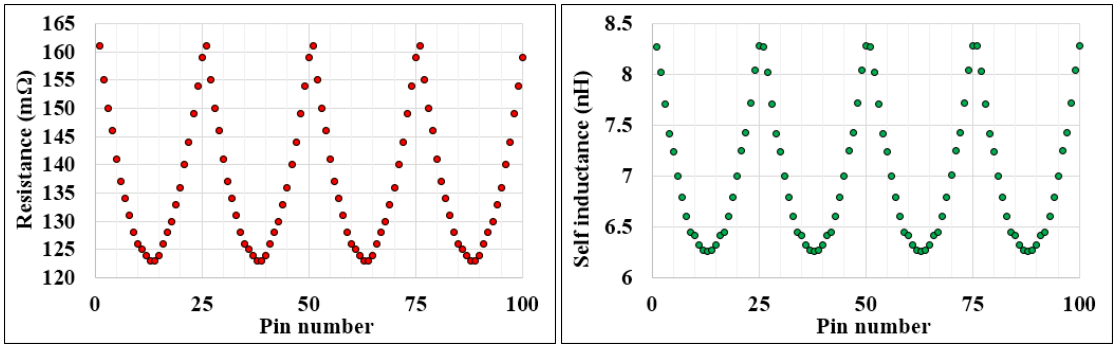


Figure 42: Open QFP100 package

The package introduces a huge number of parasitic elements. Indeed each lead frame and bonding wire has its resistivity, its capacitance with respect to the ground but also with all others, its self-inductance and a mutual inductance with all others. Parasitic elements of a generic QFP100 package was extracted with IC-EMC software [28] and plotted in Figure 43. In this package all pins are bonded with only one wire. The capacitance of each wire with respect to the ground are not represented, because it is negligible compared to parameters of the board.

Resistance and self-inductance depend on the wire length (including lead frame and bonding wire) and on its position in the package. The most influent parameter of a package regarding supplies is the self-inductance. It is in series with the one of the board and introduces a significant difference

between the VDD path and the VSS path. It contributes significantly to the common mode to differential mode conversion.



Pin resistance Pin self-inductance

Figure 43: Generic QFP100 package resistance and self-inductance

Mutual capacitance are also negligible compared to board parameters (less than 0.25pF whereas the capacitance between VDD and VSS planes is 106pF). The mutual inductance of pin 1 which is in a corner and pin 36 which is in the middle of a side with respect to all others are plotted in Figure 44.

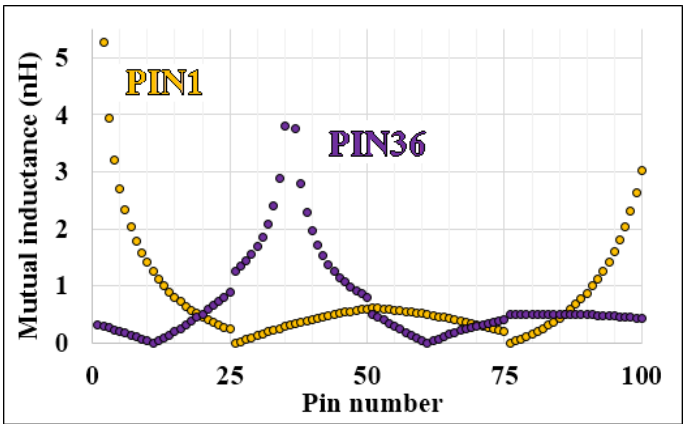


Figure 44: Package mutual inductance examples

Usually VDD and VSS wires are next to each other. It means that VDD has the maximum mutual inductance with VSS and tend to reduce the common mode to differential mode conversion.

Regarding the order of magnitudes studied in this section, the package seems to be a significant contributor to the common mode to differential mode conversion. It is valid for the same number of VDD and VSS pins and even more

if they are not equal. All those paths lead to the die and are connected to the supply of the microcontroller. The characteristics of the circuit inside the die regarding supply will be quickly described in the following part.

As usual the Table 11 summarize parameters value studied before. Here resistance are still neglected whereas is become to be significant regarding the one of the board and test bench wires. This is in anticipation to resistance value that will be seen inside the chip in the next part.

Table 11: Package RLC summary

PART		Parameter	Approximated value	Comment
PACKAGE	R	R_{pack_vdd}	140mΩ ±20 mΩ per bonding	Neglected
		R_{pack_vss}	140mΩ ±20 mΩ per bonding	Neglected
	L	L_{pack_vddn}	7nH ±1.5nH per bonding	
		L_{pack_Mutual}	6nH ±2nH if vdd close to vss	
		L_{pack_vssn}	7nH ±1.5nH per bonding	
	C	C_{pack_vdd}	<1fF	Neglected
		$C_{pack\_vdd\_vss}$	<10fF	Neglected
		C_{pack_vss}	<1fF	Neglected

3.4 Chip parameters

The chip itself can be considered as the DUT, in this case the study of the test bench stops at the package level. However a microcontroller is an assembly of several circuits. When a failure occurs, one of them is the weak element. A disturbance on supply can cause a dysfunction of a circuit, or get the supply out of its specification range and releases the security process which restarts the product.

In this part parasitic elements of the chip will not be described in details. It depends on each microcontroller. A description of a generic supply network is provided.

The supply voltage is typically 3.3V for technology under 0.35µm. Since this technological step, microcontroller's cores have a different supply voltage than IOs and Analogic circuits. The 3.3V range is still applied for IO and analogic IP, whereas the core voltage decreases with technology improvements

and reaches around 1V for 40nm technology. The low voltage can be generated from the main supply by an internal regulator or provided by the user.

The Figure 45 is a schematic representing internal power network. The analog supply is the same as the IO supply but with specific decoupling capacitor and dedicated bonding wires. 3.3V IPs are connected to power pads connection. IOs are connected to a power ring all around the die and digital IPs are supplied by a power grid by the low voltage supply. Each supply pad but the VDDA and GNDA are connected to the power ring.

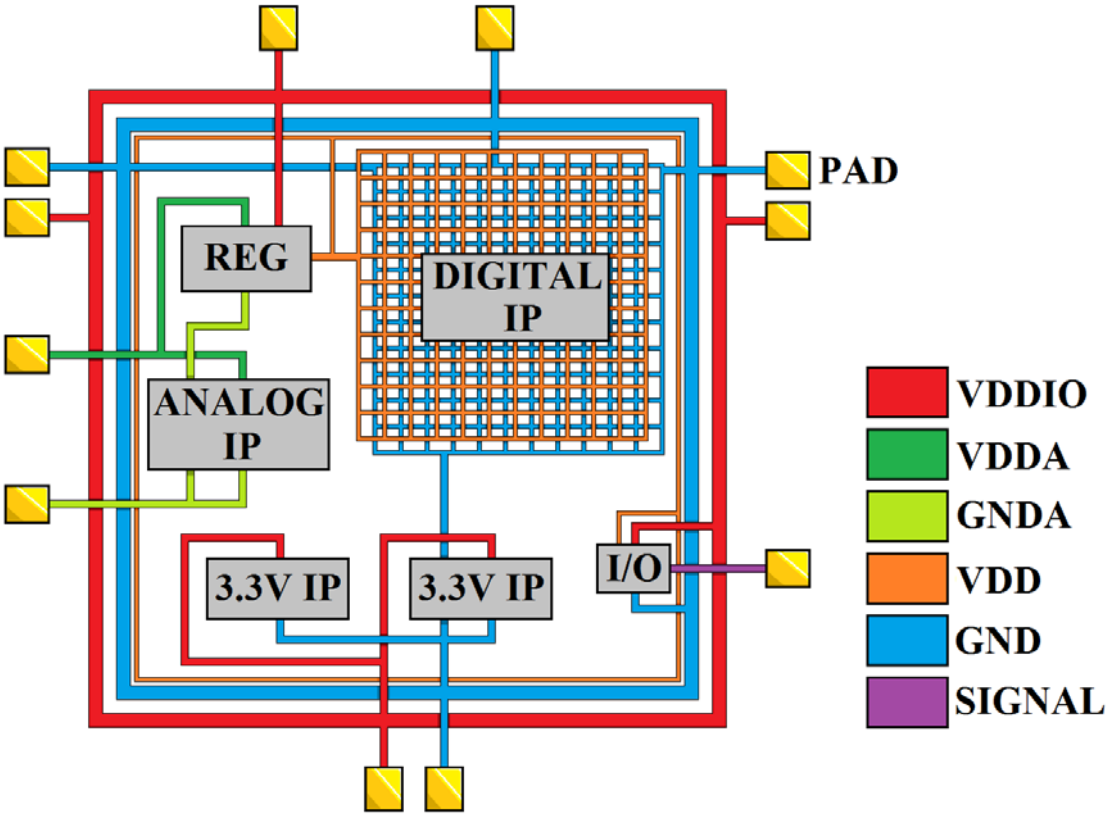


Figure 45: Power distribution schematic

The power ring is composed with several rails (VDDIO, GND and VDD). Despite that rails use several metal layer to decrease their resistivity, rail are still resistive about approximately 1Ω/mm. Its inductance depends on the die perimeter. The Digital power grid is not directly connected to the stressed supply, this is the output of a regulator. Typical parasitic elements values of main the supply are summarized in Table 12 below.

Table 12: Chip RLC summary

PART		Parameter	Approximated value	Comment
CHIP	R	R_{rail_vdd}	1Ω/mm	
		R_{rail_vss}	1Ω/mm	
	L	L_{rail_vdd}	1nH/mm	
		L_{rail_Mutual}	close to 1nH/mm	
		L_{rail_vss}	1nH/mm	
	C	$C_{die\_vdd\_gnd}$	Around 1fF	
		$C_{die\_vdd\_vss}$	few nF	
		$C_{die\_vss\_gnd}$	Around 1fF	

3.5 Nonlinear effects due to protection diodes

Protection diodes are also present in the power ring at each signal I/O it permits, among others, to participate to ESD clamp. The Figure 46 represents how they are implemented. Diodes can cause nonlinear effects on the supply differential voltage if this one reaches given condition.

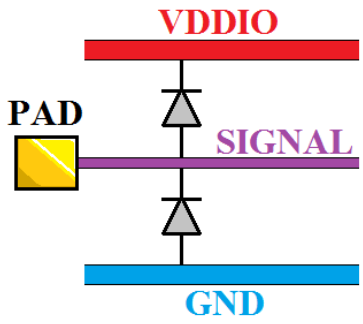


Figure 46: Protection diode on I/O

Those diodes have an effect on the signal if it goes under GND – Vd or above VDDIO + Vd and on the differential supply voltage if GND > VDDIO + 2Vd which is relatively high. Protection diodes will be neglected except if the differential supply voltage is suspected to satisfy conditions described before.

3.6 Summary

The Figure 47 represents a summary of main parameters in common mode to differential mode conversion of the stress seen before in this chapter. Only linear passive elements are considered and are summarized in Table 13. This schematic is not an accurate model designed for simulation of FTB issues. However, this is enough to provide an estimation of the frequency range significantly impacted by the common mode to differential mode conversion.

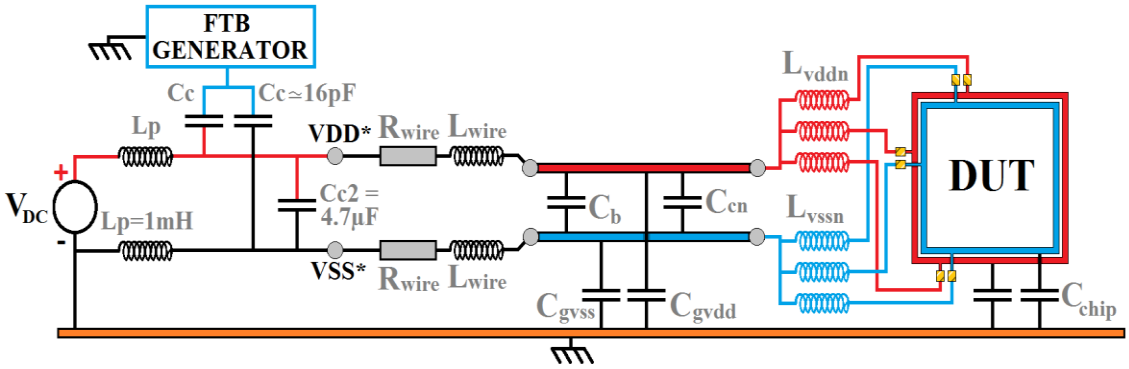


Figure 47: Main parameters summary

If the common mode to differential mode conversion is significant in a frequency range contained in the FTB stress spectrum, it could cause fails. Of course each PCB, package and chip are different but the order of magnitude of parasitic elements influencing the conversion remains in the same range.

Table 13: Global RLC summary

				Approximated value	Comment
TEST BENCH	R		R_{wire_vdd}	<5mΩ	Neglected
			R_{wire_vss}	<5mΩ	Neglected
	L		L_{wire_vdd}	100nH ±20nH	
			L_{wire_Mutual}	25nH ±15nH	Neglected
			L_{wire_vss}	100nH ±20nH	
	C		$C_{wire\_vdd\_gnd}$	<10fF	Neglected
			$C_{wire\_vdd\_vss}$	<10fF	Neglected
			$C_{wire\_vss\_gnd}$	<10fF	Neglected
BOARD	R		R_{board_vdd}	<1mΩ___	Neglected
			R_{board_vss}	<1mΩ	Neglected
	L		L_{board_vddn}	6nH ±2nH per track	
			L_{board_Mutual}	Depend on routing	Neglected
			L_{board_vssn}	6nH ±2nH per track	
	C		C_{gvdd}	2.5pF	
			C_b	100pF	
			C_{cn}	100nF per supply pair	SMD capacitor
			C_{gvss}	5pF	
PACKAGE	R		R_{pack_vdd}	140mΩ ±20 mΩ per bonding	Neglected
			R_{pack_vss}	140mΩ ±20 mΩ per bonding	Neglected
	L		L_{pack_vddn}	7nH ±1.5nH per bonding	
			L_{pack_Mutual}	6nH ±2nH if vdd close to vss	Neglected
			L_{pack_vssn}	7nH ±1.5nH per bonding	
	C		C_{pack_vdd}	<1fF	Neglected
			$C_{pack\_vdd\_vss}$	<10fF	Neglected
			C_{pack_vss}	<1fF	Neglected
CHIP	R		R_{rail_vdd}	1Ω/mm	
			R_{rail_vss}	1Ω/mm	
	L		L_{rail_vdd}	1nH/mm	
			L_{rail_Mutual}	close to 1nH/mm	
			L_{rail_vss}	1nH/mm	
	C		$C_{die\_vdd\_gnd}$	Around 1fF	
			$C_{die\_vdd\_vss}$	Globally few nF	
			$C_{die\_vss\_gnd}$	Around 1fF	

4 Common mode to differential mode conversion versus frequency

A common mode to differential mode can happens in a circuit. However, it wasn't shown in which frequency domain this conversion is significant. Thanks to the capacitance and inductance behavior of parasitic elements, we can neglect their effect in DC. To answer this question in the microcontroller case, parasitic elements sized for a typical case as in Table 14 are used to perform the simulation of the schematic of the Figure 48.

Table 14: Parasitic elements sizes for simulation

				Simulation 1	Simulation 2
TEST BENCH	L		L_{wire_vdd}	100nH	100nH
			L_{wire_vss}	110nH	110nH
BOARD	L		L_{board_vddn}	6nH/6nH/7nH	6nH/6nH/7nH
			L_{board_vssn}	6nH/6nH/6nH	6nH/6nH/6nH
	C		C_{gvdd}	2.5pF	2.5pF
			C_b	100pF	100pF
			C_{cn}	100nF per supply pair (1nH in series)	100nF per supply pair (1nH in series)
			C_{gvss}	5pF	5pF
PACKAGE	L		L_{pack_vddn}	6nH/6nH/7nH	6nH/6nH/7nH
			L_{pack_vssn}	6nH/6nH/6nH	6nH/6nH/6nH
CHIP	R		R_{rail_vdd}	1Ω/mm	1Ω/mm
			R_{rail_vss}	1Ω/mm	1Ω/mm
	L		L_{rail_vdd}	1nH/mm	1nH/mm
			L_{rail_Mutual}	close to 1nH/mm	close to 1nH/mm
			L_{rail_vss}	1nH/mm	1nH/mm
	C		$C_{die\_vdd\_gnd}$	Around 1fF	Around 1fF
			$C_{die\_vdd\_vss}$	Globally few nF	Globally few nF
			$C_{die\_vss\_gnd}$	Around 1fF	Around 1fF
			$C_{internal\_IP}$		

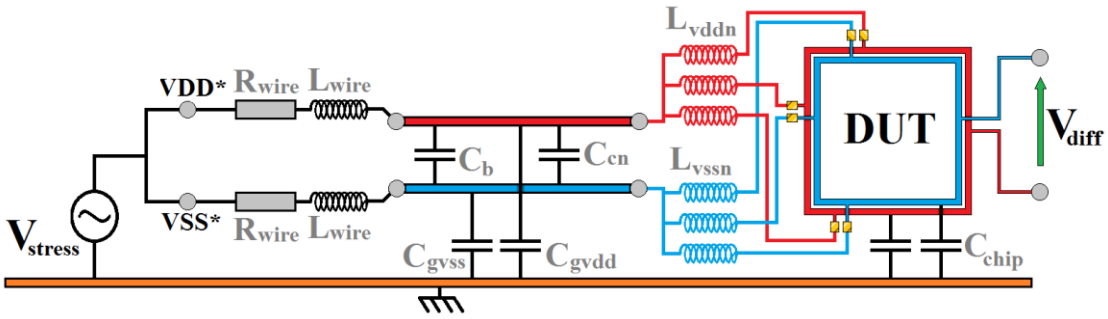


Figure 48: common mode to differential conversion global schematic

The simulation result, presented in Figure 49, shows how a common mode signal on supplies is converted into differential mode signal through parasitic elements versus frequency. As expected at low frequency, the differential mode variation is insignificant and increases with frequency. Moreover, three resonance frequencies are observable at 54.9MHz (-61dB), 257.3MHz (-30dB) and 865.5MHz (-77dB) which are peaks of common mode to differential conversion.

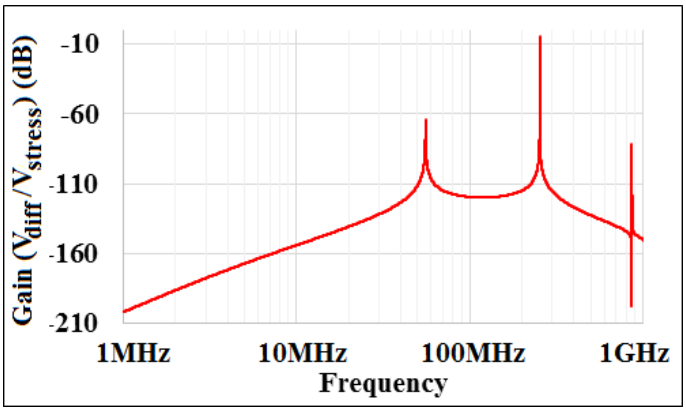


Figure 49: Common mode to differential mode conversion simulation of global schematic

Resonance peaks could be a weakness for the microcontroller if the stress spectrum contains such frequencies. For example a 1000V common mode sine amplitude applied on supplies at 54.9MHz creates a 0.9V differential mode sine inside the chip whereas the same at 257.3MHz create a 31V differential mode one. Thus, to know if the common mode to differential mode conversion is significant in the FTB case, a study of the stress itself will be done in the next section.

5 Stress shape study

The FTB stress shape is provided by the standard. This pulse is likely to excite the power network of the chip in its frequency range. The pulse repetition rate is very low, so totally out of the range of the conversion and will be neglected.

The pulse is characterized by its rise time, its fall time and its amplitude. Because it corresponds physically to a capacitor discharge through the inductive switch, the shape is described by exponential functions. The Figure 50 represents an approximation of the shape of one pulse. This signal allows us to compute easily its Fourier transform.

$$v(t) = A(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}})$$

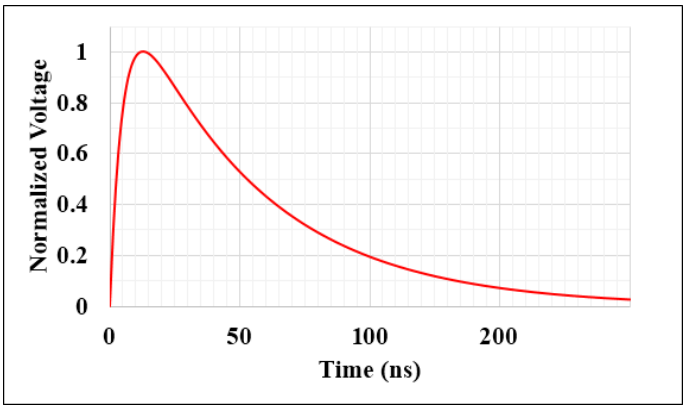


Figure 50: Stress approximation

According to the standard 61000-4-4 the rise time τ_r is 5ns and the pulse width 50ns. The Fourier transform's module of this signal is:

$$|V(f)| = \frac{A(\tau_f - \tau_r)}{\sqrt{[1 + 4\pi f^2 \tau_f^2][1 + 4\pi f^2 \tau_r^2]}}$$

Measuring the spectrum of such signal is straight forward process. Indeed the pulse measurement with spectrum analyzer provides a spectrum with uncertainty on the amplitude. The measured amplitude depends on the analyzer resolution bandwidth and the intermediate frequency filter. An empirical correction factor can be applied but here, the theoretical spectrum is used as a reference to obtain the correct amplitude value [29], [30].

Measured spectrum and theoretical spectrum are superposed in Figure 51 for 200V, and 1kV magnitude pulses.

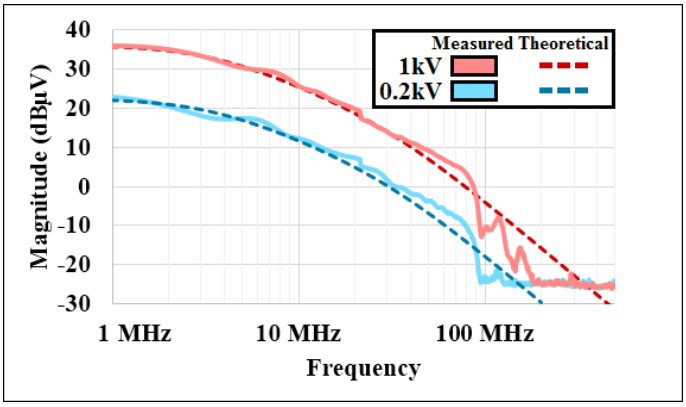


Figure 51: FTB measured versus theoretical spectrum

The measurement of the stress spectrum was performed with a spectrum analyzer connected to the FTB generator output via a 60dB attenuator to protect the analyzer. The FTB generator output is also connected to a test bench (coupling capacitor and test board) in order to apply a load corresponding to a normal test. No measurement was performed above 1kV but the stress amplitude can reach 3.5kV during the test.

Regarding the FTB stress spectrum, for the next sections of this document, analysis of the frequency response of the power network will be done below 1GHz.

6 Conclusion

The FTB disturbance is a common mode stress on supply. A real common mode perturbation on supply cannot disturb an electrical circuit, but it was seen that it can be transformed into differential mode disturbance. The difference of VDD and VSS paths due to parasitic elements is the cause of the common mode to differential mode conversion. The entire test bench was analyzed to provide the order of magnitude of supply network parasitic elements.

The order of magnitudes extracted from this study permitted to build a simple model able to provide a first order frequency response of the power network when it is submitted to a common mode variation. The stress itself was also studied, and its frequency spectrum extracted. The comparison between the stress injected during the FTB test and the frequency response of the power network shows that the common mode to differential mode can be significant in the frequency range of the stress.

The next part is dedicated methodology using observed stress propagation path to help investigation.

Chapter 3 Power network analysis methods

The FTB stress in common mode applied to supply wires might not be an issue for electrical circuits in a chip, but observations show how microcontrollers can fail to this test. The most relevant hypothesis is that the common mode is transformed into differential mode during a FTB stress due to the difference between the power path and ground path from the stress injection point to the tested circuit. The difference between the two paths was studied to provide order of magnitude and so a sensitive frequency range. The order of magnitude of parasitic elements allows a significant common mode to differential mode conversion in the stress spectrum frequency range. It was also seen that resonance phenomenon can occur and create a weakness.

This chapter will firstly study in details the power network and the resonance phenomenon. Finally new methods for the study of the stress propagation inside the chip will be proposed. In all, three methods will be presented, the global resonance analysis, the conduced emission and near field measurement method.

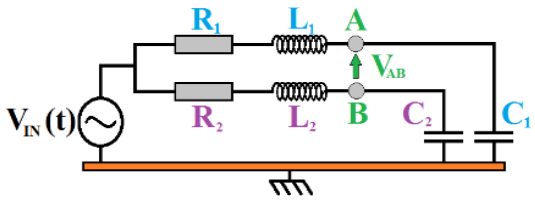
1 Power network behavior

Collecting information on the power network frequency response could be a huge help for debugging purpose. Indeed the power network was identified to be the main contributor in the FTB test results. It can protects weak circuit from the disturbance but also amplifies it. Understanding its behavior is required for investigations.

1.1 Resonances and FTB disturbance

When the stress propagates in the two different VDD and VSS paths, a resonance on one of those path creates a big amplitude difference at the resonance frequency. And so, the common mode to differential mode conversion is amplified at their resonance frequency.

The FTB disturbance is a pulse, the supply network will react to it with its pulse response. Of course, the stress is not a pure delta function, so the pulse response of the network is limited to excitation frequency contained in the disturbance. Thus, the supply network reacts as a piano string hit by a hammer, it vibrates with its proper frequencies. The Figure 52 shows the behavior of two simple RLC paths excited by a FTB disturbance.



$R_1=R_2= 2\Omega$

$C_1=C_2= 2pF$

$L_1=10nH\ L_2=12nH$

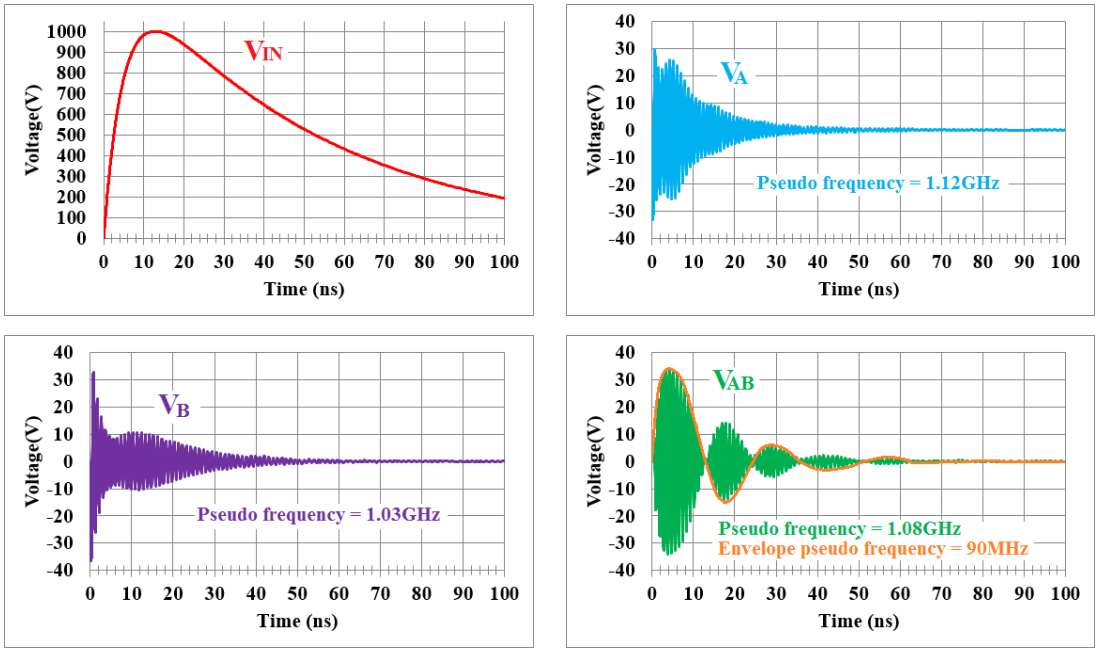


Figure 52: Two RLC circuit excited by an FTB stress simulation

Considering V_A and V_B as perfect sine wave (with no damping):

$$V_A = \sin(2\pi f_{0A} t)$$

$$V_B = \sin(2\pi f_{0B} t)$$

Then:

$$V_{AB} = V_A - V_B = 2\sin\left(\frac{(f_{0B} + f_{0A})2\pi t}{2}\right).\sin\left(\frac{(f_{0A} - f_{0B})2\pi t}{2}\right)$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \Rightarrow f_{0A} = 1.12GHz \text{ and } f_{0B} = 1.03GHz$$

It is possible to identify a carrier wave and an envelope. The envelope corresponds to the lower frequency sine which is the one at the frequency $\frac{f_{0A}-f_{0B}}{2}$. The sine carrier is at the frequency $\frac{f_{0A}+f_{0B}}{2}$.

The Table 15 shows different configurations and their stress response characteristics. Only one parameter changes from one row to the other. Pf corresponds to the pseudo carrier frequency, Ef to the envelop frequency and A the maximum amplitude of the system response.

Table 15: Stress response characteristics versus R L and C values

R_1	R_2	C_1	C_2	L_1	L_2	Pf	Ef	A
2Ω	2Ω	2pF	2pF	10nH	12nH	1.08GHz	90MHz	35V
2Ω	2Ω	2pF	2pF	20nH	24nH	0.77GHz	66MHz	75V
2Ω	2Ω	20pF	24pF	10nH	10nH	0.33GHz	33MHz	76V
1Ω	2Ω	2pF	2pF	10nH	10nH	1.12GHz	No	8.5V
1Ω	1Ω	1pF	1pF	1nH	1.5nH	4.65GHz	1GHz	13V

When the two parallel RLC paths are excited by the FTB stress, they resonate at their proper frequency. The differential mode resonance frequencies is not the same as the resonance frequencies of each path but depends on it. Computing is easy on the chosen example, but the power network is much more complex. The power and the ground path are not identical as they have their own proper frequencies when they are excited in common mode. There is no chance that resonance frequencies of the power path are the same as the ground

path. Later in this chapter a new analysis method will be developed to identify resonance frequencies of the power network.

1.2 Pulse response measurement

The power network stress response is not measurable during the FTB stress for different reasons. Firstly, the FTB stress disturbs the measurement by coupling on cables. Secondly, the measurement point should be inside the chip and makes it much more complex.

The supply network can be considered as a linear invariant system if diode effects are neglected. So the Fourier transform of its pulse response corresponds to its transfer function. It means that knowing the transfer function of the power network between the stress injection point and the tested circuit inside the chip permits to know how it behaves to the FTB stress.

It is possible to measure the transfer function by another mean than the pulse response. Indeed measuring the output amplitude of a system for each frequency with a unity amplitude input allows also to obtain its transfer function (cf. Figure 53). By this way, the coupling on cable due to the huge amplitude pulse can be avoided.

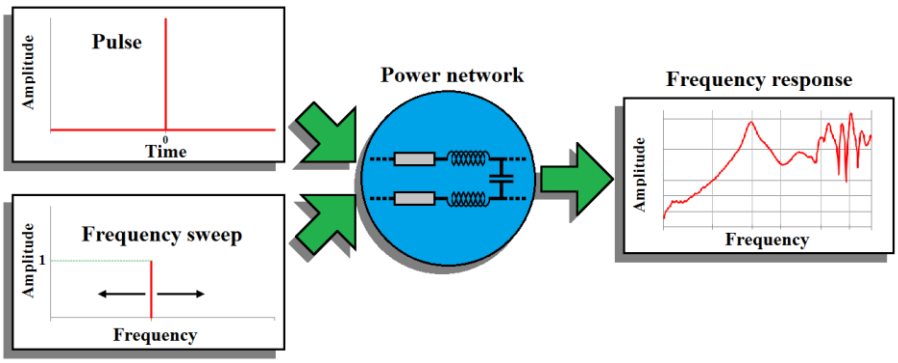


Figure 53: Two ways providing frequency response of an invariant linear system

The power network output is still not accessible. Performing probe tips measurement is possible but not applicable easily in the FTB test conditions. Another way to measure the output of the supply network is required. The next

section introduces RLC resonance specificities to determine how it can be used to collect information on supply network.

1.3 RLC network resonance specificities

A supply network is mainly made of simple metal path in addition to decoupling capacitors. Metal path like wire, PCB routing or silicon routing can be modeled as RLC structures. The extraction of such stray elements was introduced in the previous chapter. Those structures made of passive linear components can be resonant. A first analysis of a simple RLC series circuit will help to understand the resonance phenomenon and will be generalized to more complex structures.

In a serial RLC circuit like illustrated in Figure 54, the resonance frequency F_0 happens when the reactance of the inductor is equal to the reactance of the capacitor $X_L = X_C$, the impedance of the circuit is equal to R.

$$F_0 = \frac{1}{2\pi\sqrt{LC}}$$

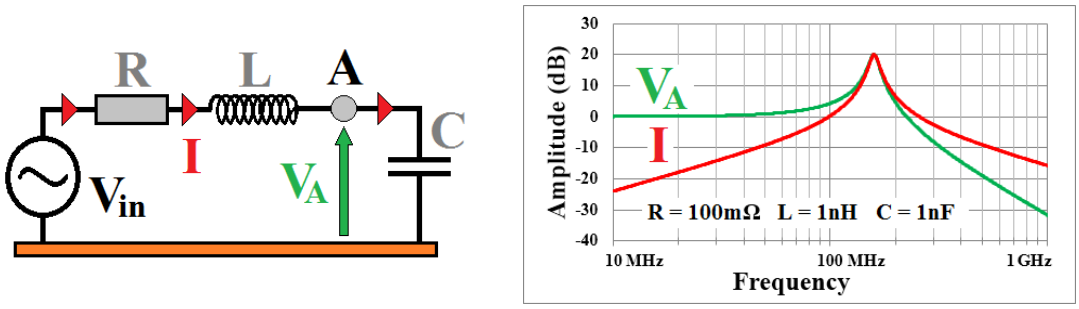


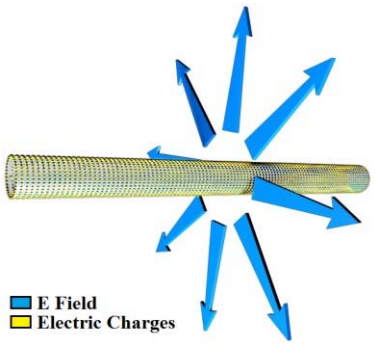
Figure 54: Serial RLC

At this frequency, the voltage V_A and the current I are at their maximum. The magnetic field depends on the current in the wire, and the electric field on the voltage. The resonance frequency of a serial RLC circuit corresponds also to a maximum of radiated electromagnetic field. The Figure 55 shows how near electric and magnetic fields are around the conductor and gives their amplitude formulas.

$$E = \frac{q}{2\pi r \varepsilon_0}$$

Where:

- E is the value of the electric field in V/m
- r is the distance from the wire
- ε_0 is the permittivity of free space
- q is the charge per length unit



$$B = \frac{\mu_0 I}{2\pi r}$$

Where:

- B is the value of the magnetic field in Tesla
- r is the distance from the wire
- μ_0 is the permeability of free space
- I is the current passing through the wire

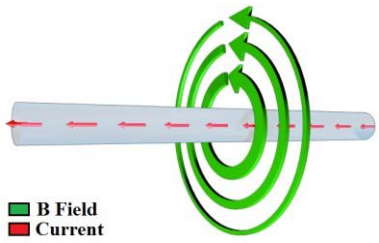


Figure 55: Electric and Magnetic fields

Circuits with more than one inductor and capacitor have several resonance frequencies. The calculation of their resonance frequency is very complex. For such circuit, the simulation will be used. An example is given in Figure 56 with 3 cascaded serial RLC circuits. It is possible to observe 3 resonance frequencies, one for each LC structure.

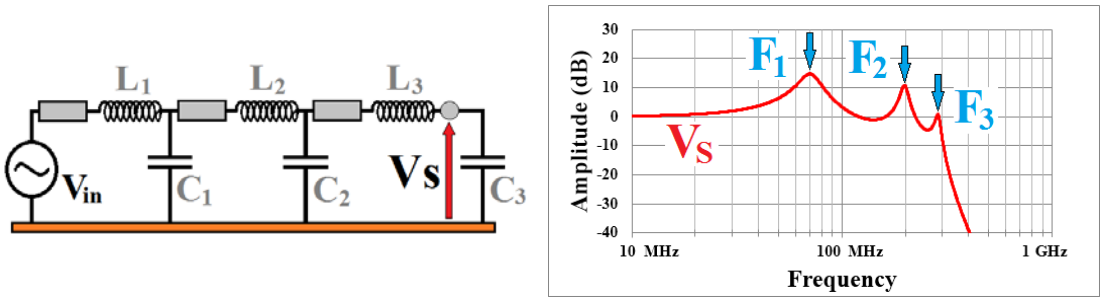


Figure 56: 3 cascaded RLC circuits

The same phenomenon occurs on complex structures such as power network. At some frequencies a maximum of power passes through it, whereas it is filtered at other frequencies.

2 Resonance analysis methods

It was shown that it is possible to measure the pulse response of a system by a convoluted way. Indeed measuring for each frequency the output of a system whereas a unit amplitude sine wave is applied on the input permits to obtain the transfer function module of a system and so its pulse response.

In the case of the microcontroller supply network, the output of the system is not accessible. Using an embedded measurement circuit is not excluded. This kind of measurement circuit has already been developed in the past [27] [28] but are not adapted to the measurement of a pulse in common mode on supply. Nevertheless, the focus is put on noninvasive measurement method applicable on all products with no silicon surface needs.

It was demonstrated that resonances can be a weakness for the device under test. It was also seen that when a resonance occurs, an electromagnetic emission pic happens as well. Methods were developed to measure resonance frequencies of the supply network using electromagnetic like illustrated in Figure 57 or conducted emission as the output of the system.

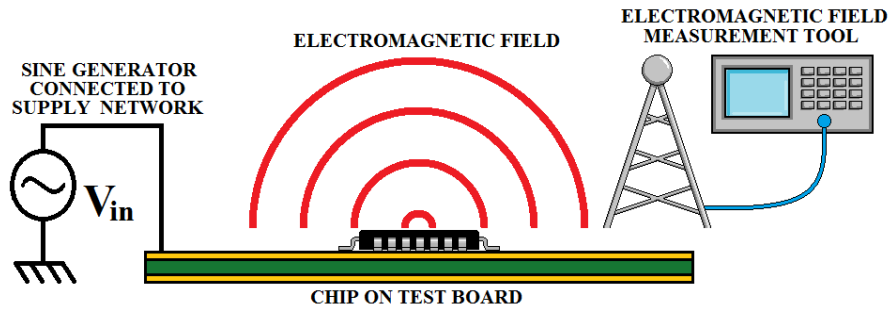


Figure 57: Supply network electromagnetic field measurement principle

In a first time the principle of the methodology will be presented. Simple circuits will be analyzed and simulated in order to validate the methodology. Finally, a microcontroller will be analyzed using resonance analysis methods. During this test the amplitude of V_{in} is chosen to assume that its value is under the transistor threshold (the chip is off), typically few mV.

2.1 Global resonance analysis method

Because a resonance frequency of a RLC structure corresponds to an electromagnetic radiation peak, it is possible to identify them by measuring their radiated electromagnetic field. By this way, the power network can be globally measured by a noninvasive method. The TEM Cell [33] is a tool usually used for chip emission measurement, which permits to measure both electric field and magnetic field at the same time. For the proposed methodology, the power network is excited by a low amplitude sine and the electromagnetic field of the power network is measured by a spectrum analyzer via a TEM Cell. The Figure 58 illustrates the measurement set up.

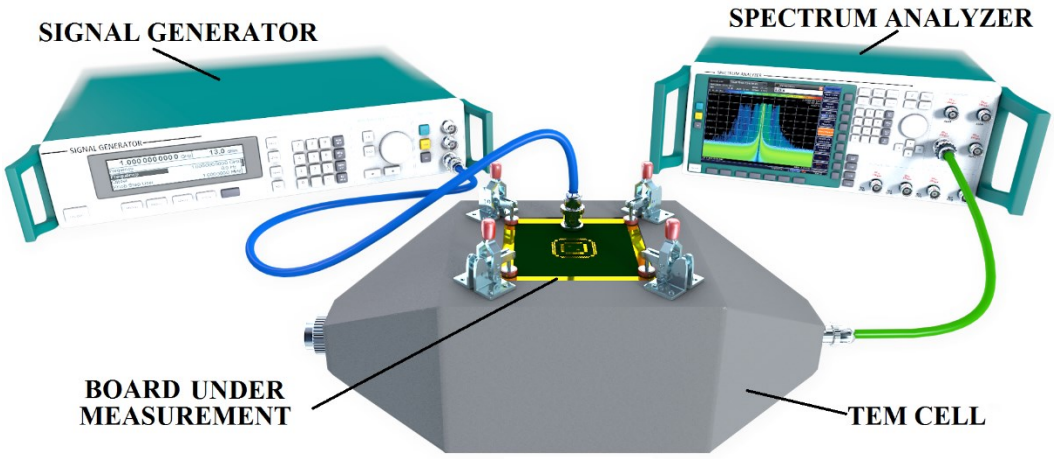


Figure 58: Resonance analysis measurement bench

To perform the measurement, the sine frequency sweeps the desired range. The analyzer keeps the envelope of the spectrum in memory thanks to the "maxhold" function. Because the magnetic field must be perpendicular to the septum to be measured, the operation must be done with two orientations of the board, one turned about 90° with respect to the other. The TEM Cell can be replaced by any tool which permits to measure the electromagnetic field depending on the size of the device under measurement and the frequency range. In this section a TEM Cell and a GTEM Cell will be used.

2.1.1 Measurement bench validation with simple circuits

In order to validate the resonance analysis measurement bench, simple RLC structures were measured and simulated. Those RLC structures are implemented on a test board compatible with a TEM Cell and with the same dimensions as FTB test board. First order simulation using lumped element model are performed to correlate the first resonance frequency with the measurement results.

2.1.1.1 A simple wire

The first circuit is a simple metal wire which is connected on both sides of a two layers PCB. The input signal is applied between the two planes, and the PCB is placed in the TEM Cell. The Figure 59 describes the board and its dimensions as well as its first order electric model.

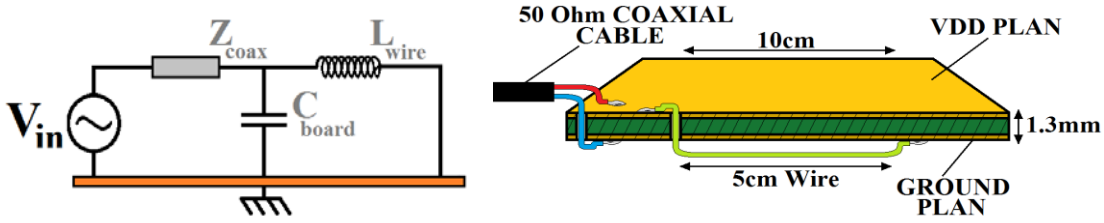


Figure 59: Simple wire board setup

The main capacitance is between the two layers of the PCB and can be easily evaluated with the following formula:

$$C_{board} = \frac{\varepsilon_0 \varepsilon_r S_{board}}{d} = \frac{8.85.10^{-12}\ 3.6\ .100.10^{-4}}{1.3.10^{-3}} = 200pF$$

$Z_{coax} = 50\Omega, \mathrm{L_{wire}} = 50\mathrm{nH}$ (with $1\mathrm{m} = 1\mu\mathrm{H}$ approximation), $\mathrm{R_{wire}}$ is neglected

The permittivity of the board ε_e=3 can change depending on the board material. This model in Figure 59 permits to extract the resonance frequency, to fit with the measurement results, the TEM Cell must be modelled too.

TEM Cell and GTEM Cell models

Both TEM Cell and GTEM Cell models are presented in Figure 60, they provide the same results in measurement and simulation but the GTEM Cell allows measurement at higher frequencies.

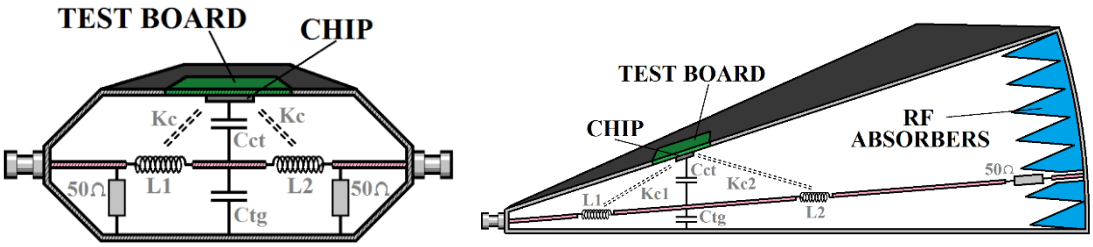


Figure 60: TEM Cell and GTEM Cell electrical spice simulation model

A TEM Cell [34][35] is made of an external sheath connected to the ground and a central conductor called septum which is electrically coupled to the circuit under measurement. The electric field coupling is modelled by a capacitor C_{ct} between a node of the circuit and the septum. The magnetic field coupling is modelled by a mutual inductance K_c between wires in the device under test and the septum. There is a coupling between each node of the measured circuit and the septum which can be represented by an infinity of capacitors and mutual inductance. Their value depends on the geometry of the circuit and its placement with respect to the septum.

The TEM Cell is symmetric so the inductive representation of the septum L_1 and L_2 are equal whereas for the GTEM Cell $L_2 \approx 10 \times L_1$. The septum is designed to have a characteristic impedance of 50Ω whatever the TEM Cell.

$$\sqrt{\frac{L1 + L2}{C_{tg}}} = 50\Omega$$

When a SPICE simulation is performed, each node of the circuit is coupled to the septum but the value of the coupling parameter K_c or C_{ct} is adjusted to fit the measurement magnitude. Those values do not change resonance frequencies.

The measurement using a GTEM Cell and simulation results are superposed in the Figure 61 and correspond to the theoretical resonance frequency.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 50MHz$$

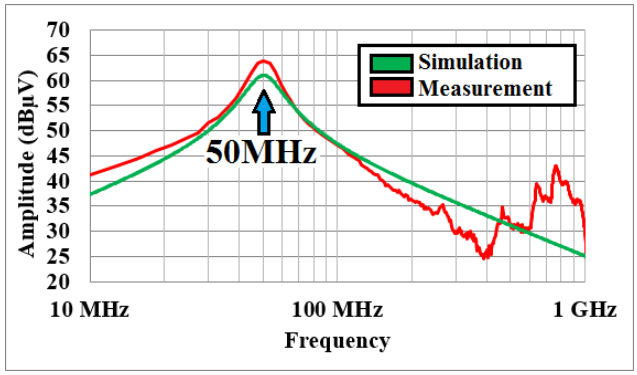


Figure 61: Simple wire resonance analysis simulation and measurement

Because it is a simple circuit only one orientation of the board is analyzed. Indeed the septum parallel to the wire is the optimal position.

Other resonance frequencies appear in the measurement results which are not modeled. Indeed the first order lumped element model does not permits to reproduce it.

2.1.1.2 Double wires

A second circuit with more complex structure is measured. The PCB is the same as the previous with two parallel wires welded on it instead of one. This configuration introduces a coupling factor between inductance which increase the total equivalent inductance compared with two independent wires.

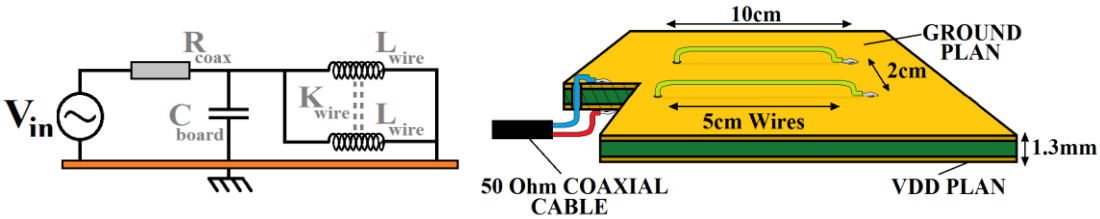


Figure 62: Double wires board setup equivalent circuit

The board capacitance is the same as the simple wire board as well as wire inductance but reproduced two times. The mutual inductance for two

parallel wires when the current flows in the same direction $M_{\uparrow\uparrow}$ can be evaluated with the following formula:

$$M_{\uparrow\uparrow} = \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l} \right] = 12nH$$

Where:

- l is the wire length
- d is the distance between wires

This time the equivalent inductance depends on the wire length, but also on the distance between wires. The theoretical equivalent inductance of those two parallel wires which allow to calculate the resonance frequency is:

$$L_{eq} = \frac{L_1 L_2 - M_{\uparrow\uparrow}^2}{L_1 + L_2 - 2M_{\uparrow\uparrow}} = 30nH$$

$$\Longrightarrow f_0 = \frac{1}{2\pi\sqrt{L_{eq}C}} = 64MHz$$

Measurement and simulation results are represented in the Figure 63 below. As well as the one wire board, only one orientation, with wires parallel to the septum is analyzed. There is a good correlation between simulation, measurement and theoretical calculation regarding the first resonance frequency.

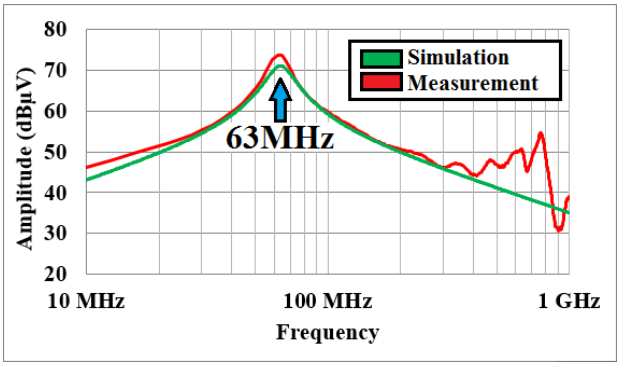


Figure 63: Double wires resonance analysis simulation and measurement

The mutual inductance tends to decrease resonance frequency compared with a model without it. Indeed the more the two wires in which the current flows in the same direction are close to each other the more they behave as one wire alone.

Usually the two wires of supply pairs are as close as possible to decrease electromagnetic radiation and reduce the inductance value in differential mode. It means that in common mode those two wires tend to behave as one (this is the case of a wire bonding supply pair in a package for example).

Those examples, of course simple allow to validate the measurement method. It is possible now to analyze more complex circuit such as a microcontroller. Analysis may take into account the differential mode and the common mode to differential mode conversion.

2.2 Microcontroller measurement

2.2.1 Differential mode resonance analysis

This methodology can be applied on a microcontroller. The device is not powered and the sinusoid is applied between the test board VSS and VDD nets. It means that the analysis is in differential mode at the supply connection of the board. The amplitude of the stress signal is under transistors and diodes thresholds in order to have less distortion as possible. The sinusoid frequency sweeps in the desired range and the radiated electromagnetic field is measured by a spectrum analyzer via a TEM Cell. The Figure 64 shows the results of a resonance analysis of a microcontroller from STM32FXX family in a QFP100 package.

A first resonance frequency happens near 300MHz and corresponds to a maximum power transmission of the stress inside the chip. This resonance frequency can be a weakness for the microcontroller.

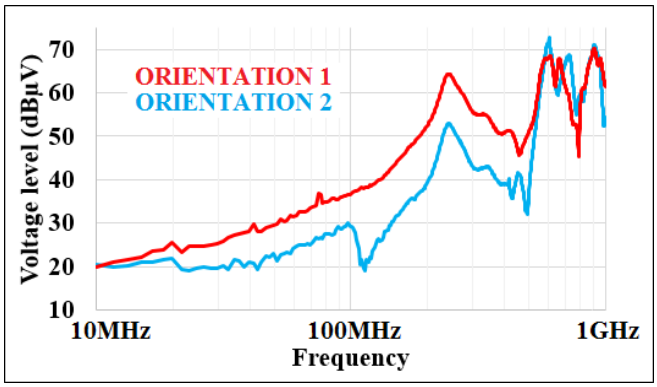


Figure 64: Microcontroller differential mode resonance analysis example

For shielding purpose the PCB used for the TEM Cell measurement closes the TEM Cell with its ground plane. By this way only the chip with its package is measured. But this configuration makes the common mode measurement impossible. Indeed the PCB ground plane voltage must vary with respect to the ground of the TEM Cell and measurement tools. In this configuration only resonance of the power network stressed in differential mode is measured. This is correct if we consider that there is a differential mode stress at the input of the PCB, but it was seen before that the PCB and the package contribute also to the common mode to differential mode conversion. This measure is not enough to show common mode to differential mode resonances. A common mode measurement is necessary to know resonance frequency of the system when it is subject to FTB stress.

2.2.2 Common mode resonance analysis

A common mode measurement setup, illustrated in Figure 65, was also developed. Compared to the previous setup, a one layer PCB is added between the test board and the TEM Cell. This PCB isolates the TEM Cell ground from the VSS layer of the test board. This PCB is also used to close the TEM Cell shielding and limits the capacitive coupling between the test board VSS layer and the TEM Cell septum.

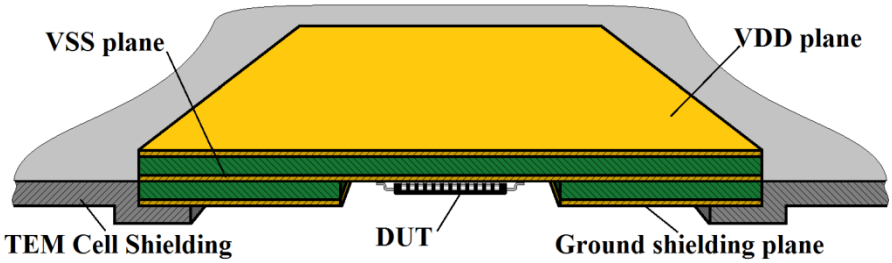


Figure 65: Common mode TEM Cell measurement

This setup allows to get the emission of the chip when a common mode excitation is applied on its supply. The VSS plane does not contribute to shielding anymore and emits also electromagnetic field. The coupling between the VSS plane and the TEM Cell septum is mainly capacitive and significant. The electric field emitted by the VSS dominates the magnetic field generated by the current in the package.

Both global investigation methods, common mode and differential mode, provide a result which allows to distinguish main resonance frequencies. In the differential mode measurement setup, the excitation is less representative of the FTB disturbance. But it was seen before that when one of VDD or VSS path resonates, the common mode to differential mode conversion is amplified. As a consequence, when a differential mode resonance occurs it is very likely that a resonance happens also in common mode. It is visible here by observing the resonance around 200MHz in Figure 64 which is also present in common mode in Figure 66 orientation 1. By this way, the behavior of the power network is not well reproduced but this method gives important trails for investigations.

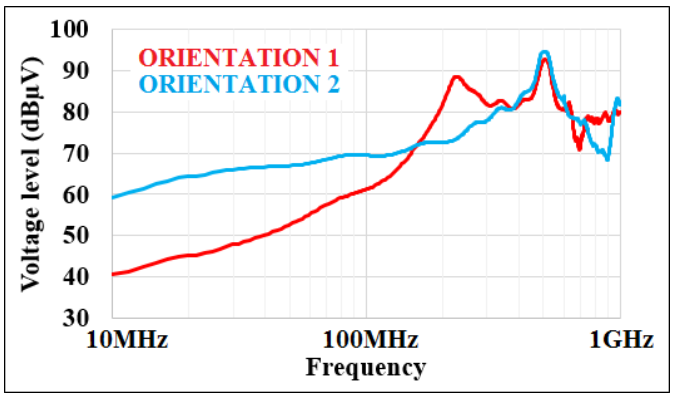


Figure 66: Common mode measurement setup result

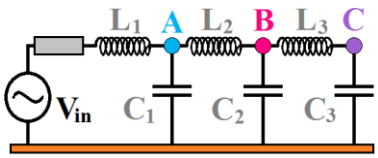
The common mode method excitation is more close to the FTB test. But the drawbacks are that the TEM Cell is not adapted for such measurement, and a common mode current and voltage disturb the measurement result. This method can be used in complement to the differential mode method to correlate results and confirm some resonance frequencies.

2.3 Local resonances analysis methods

The global resonance analysis methodology allows to know a resonance frequency of the power network. Because the TEM Cell measures the global electromagnetic field radiated by the chip, it is not possible to know where the resonance is spatially localized in the chip. Before starting the description of local resonance analysis benches, the local resonance phenomenon will be introduced.

2.3.1 Local resonances

Resonance of order up than one can involve nodes and antinodes. A simple example is illustrated in Figure 67 where a 3th order RLC structure and its frequency response are depicted. In the graphic, there are two representations of same data, the classic curve of the amplitude versus frequency, and another which allows to see more easily the spatial distribution of the voltage amplitude.



In this example:

$L_1=L_2=L_3=5nH$

$C_1=C_2=C_3=200pF$

And $R = 1\Omega$

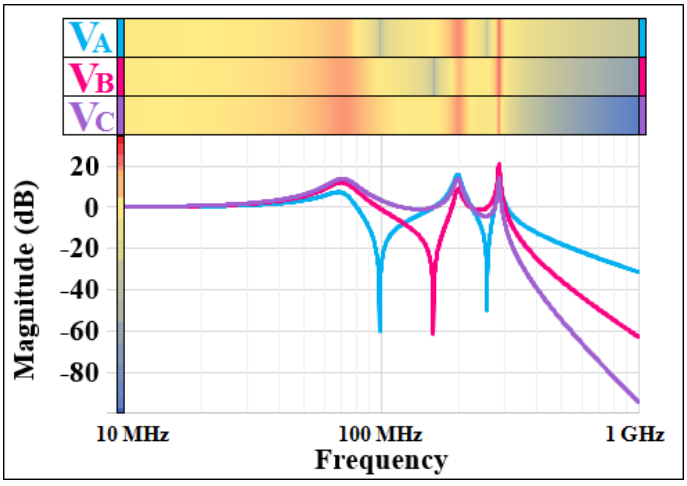


Figure 67: Local resonance illustration

A power network can be modelled as a complex RLC structure as well, the same local resonance phenomenon happens in it. A measurement bench using conducted emission was implemented to evaluate the amplitude of this phenomenon in the microcontroller case.

2.3.2 Local resonance measurement bench

2.3.2.1 Conducted emission measurement bench

In a microcontroller the power ring dispatches the supply to all IOs around the chip like described in Figure 45 (page 49). It is possible to observe the value of the supply in the power ring when a '1' is set on an IO buffer. This technique is already used in the EMC standard IEC 61967-4 [36], which deals with the conducted emission of a product.

A test board dedicated to IEC 61967-4 standard illustrated in Figure 68 will be used to perform the power ring local resonance measurement.

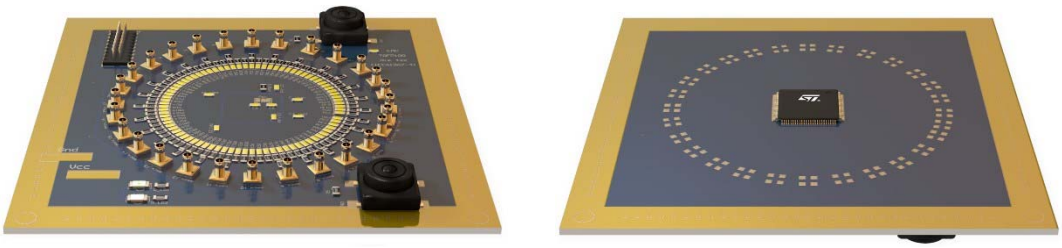


Figure 68: Conducted emission board

A High pass filter is applied on each output to avoid the DC voltage, and IOs are grouped by 3 for board space saving purpose. The simulated frequency response of the High pass filter is given in Figure 69. Its -3 dB cut off frequency is 100 kHz and the local resonance measurement will focus in the 10MHz to 1GHz frequency range which is in the filter bandwidth.

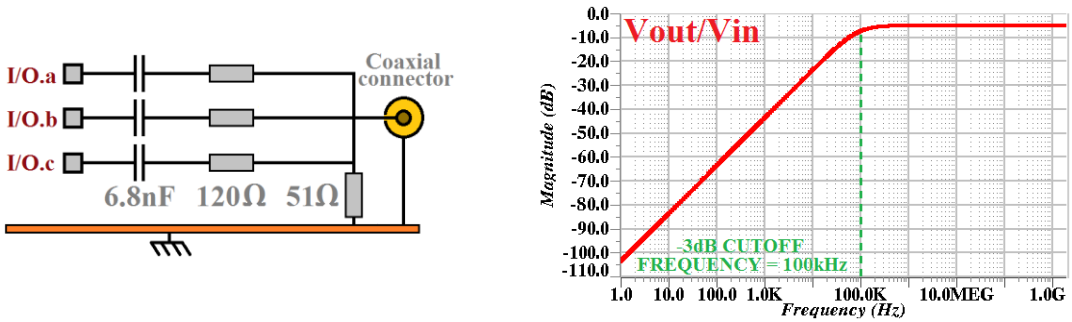


Figure 69: Conducted emission board high pass filter

This board is made for QFP100 package and 27 measurement points are available around the power ring. Each of those measurement input is equipped with a SMB connector. It was checked that the IO buffer does not filter the signal in the measurement frequency range. The Figure 70 shows its power ring to output frequency characteristic. The -3dB cut off frequency of this filter is 7GHz whereas the wanted measurement stops at 1GHz.

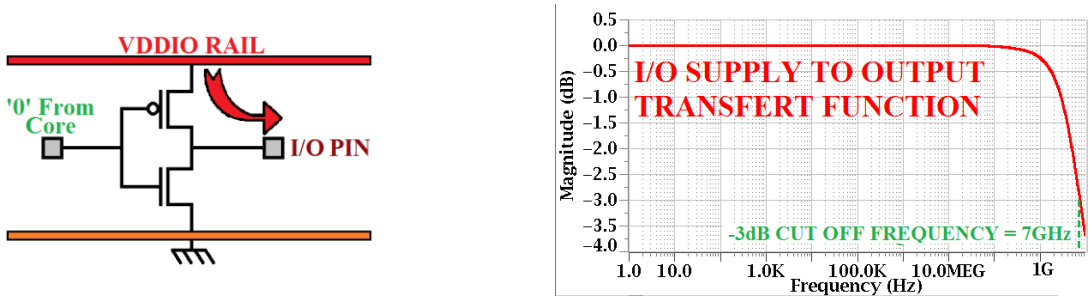


Figure 70: IO buffer Vddio to output filter characteristic

The local resonance measurement bench is presented in the schematic Figure 71. A sine wave signal is introduced on supply via the FTB test capacitive coupler. It means that the variations are in common mode. The microcontroller is running and the applied sine amplitude is higher than the microcontroller noise, but still under transistors threshold. By this way, the measurement is not disturbed by the microcontroller activity. The frequency sweeps in the 10MHz to 1GHz range and the output magnitude is measured via a spectrum analyzer for each IO group.

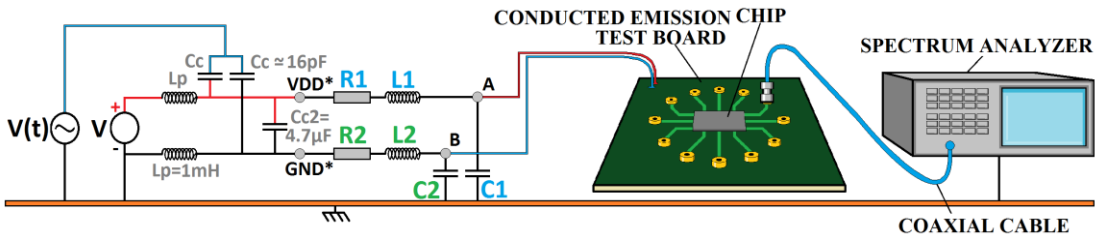


Figure 71: Conducted emission measurement test setup

Measurement results of each IO group are plotted in a same chart represented in Figure 72. This way of representation allows to easily locate spatial resonances. The vertical axis represents the IO group number shown in the schematic on the left side. Because it is a ring, the IO group number 27 is next to the IO Group number 1. Notice that the frequency axis is not logarithmic but linear.

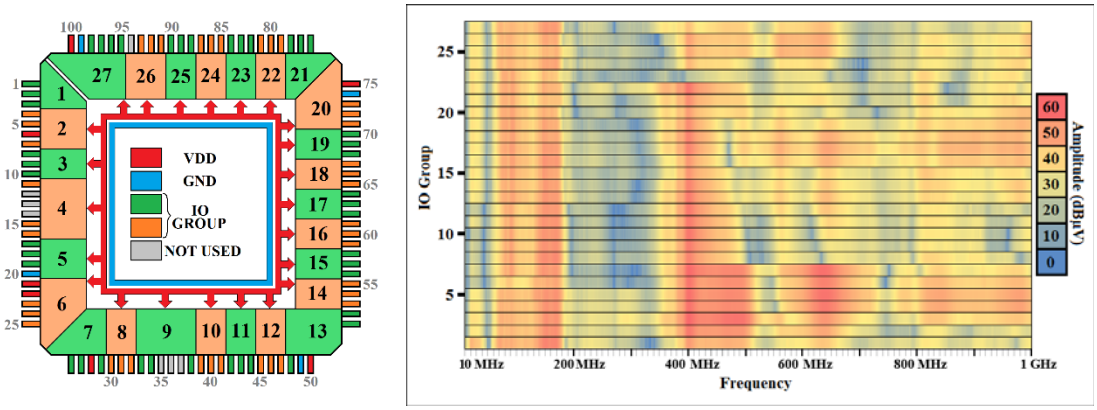


Figure 72: Local resonance measurement result example

The first resonance, around 100MHz, happens all around the power ring. For next resonances, the more the frequency increases, the more the power ring is heterogeneous. It is true for the power ring and it is also true for the entire power network. Considering that, depending on the stress frequency, a susceptible circuit could be immunized if it is placed on a resonance node like IO group 23. Indeed, all IOs are red, in Figure 72, at 400 MHz, except the IO group 23, which is blue.

Notice that an intuitive hypothesis is that if the wavelength of the signal is much higher than the circuit length, the voltage is homogeneous in conductors. The wavelength of a 1GHz signal is about 30cm which is much

longer than a chip, but local resonances are clearly present. This is due to the capacitance and inductance spread on the power network which make the propagation delay of signal non negligible with respect to the signal period.

Observation effect

Observing the power ring with this method changes its frequency response. Indeed when the supply is observed through an IO, the IO bonding wire from the pad to the observation pin is added to the power network. It disturbs the measurement but also changes the power network resonance frequency by adding a non-negligible inductance to it.

Another drawback of this method is that the differential mode is observed with the board ground plane as a reference. So the observed voltage is not exactly the internal differential variation. But, if we consider the board ground plane as perfect, the measured voltage corresponds to internal nodes with respect to the ground.

This method needs to be carefully set up in order to be as close as possible to the application case, for example by output a '1' on IO used in the real case. It limits the observation point but keeps the power network as it is during the application. It can be very useful in investigation process because, compared to resonance analysis, it is independent from coupling factor between the TEM Cell and the microcontroller's power network.

Another method is presented in the next part allowing to identify resonance area. It uses a near field scan bench to measure the field emitted above the power network.

2.3.2.2 Near field measurement bench

The principle of the near field measurement bench is to use a XYZ table to move a near field probe above the device under test. It allows to map the generated field with a good spatial accuracy. The probe sweeps an array of measurement point above the device under test. The x and y step shown in Figure 73 and the probe size determines the spatial accuracy.

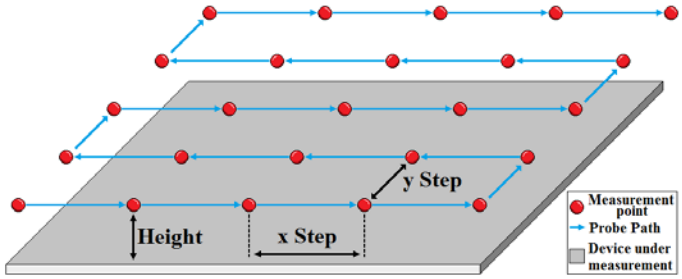


Figure 73: Probe measurement path

A spectrum analyzer collects electromagnetic field amplitude value through the probe in the desired frequency range. A computer supervises the measurement bench and put measurement points in a file to visualize results. The bench schematic is depicted in Figure 74.

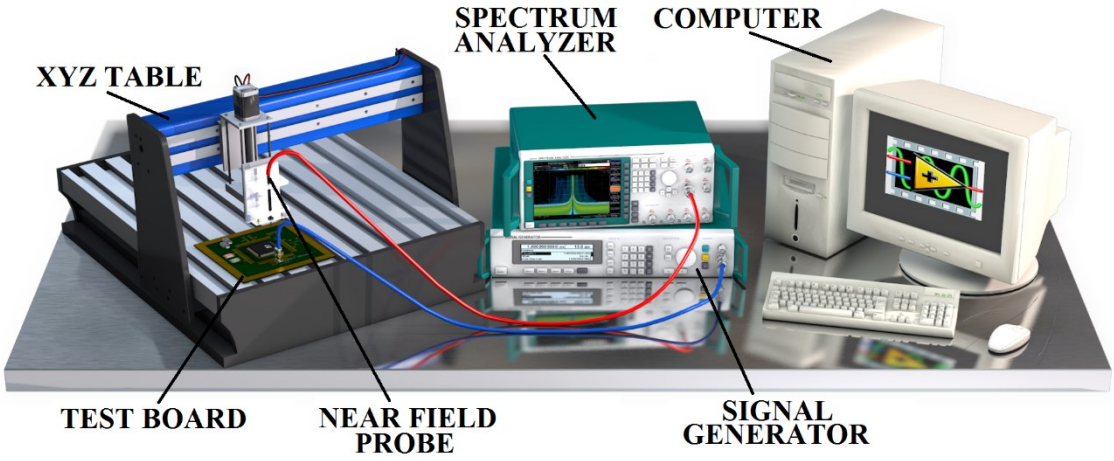


Figure 74: Near field measurement bench

The measurement principle is the same as the resonance analysis bench but a near field probe replaces the TEM Cell. The power network is excited by a low amplitude sine and the electromagnetic field of the power network is measured by a spectrum analyzer via a near field probe. The sweep time of the XYZ table is very long (approximately 20 measurement points per minute), but the measurement method brings more information on resonance locations. This bench allows Electric or Magnetic field measurement depending on the probe. Magnetic and electric probes are described in Figure 75 and Figure 76. Choosing the kind of field is a huge advantage because it is possible, for example, to avoid electric field which is mainly generated by the common mode variation.

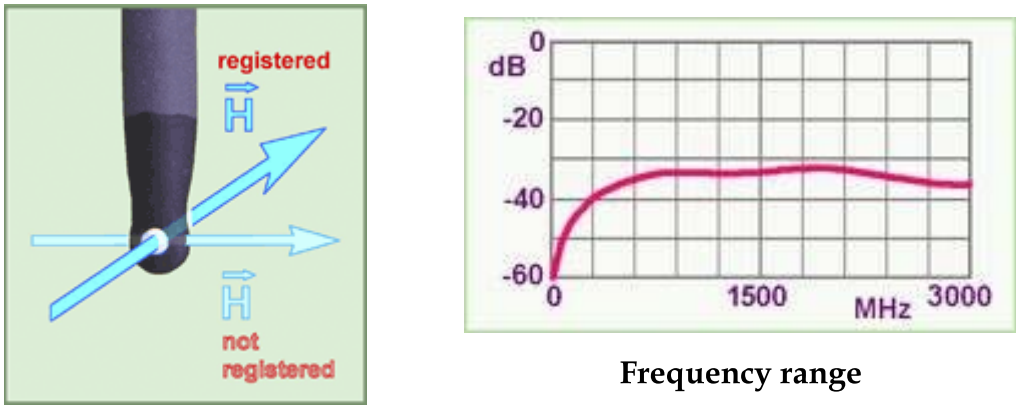


Figure 75: Langer Magnetic field probe [37]

This probe allows the measurement of the magnetic field. This is a coaxial probe based on the Lenz's law [38]. By making a loop between the copper core and the copper shield the magnetic flux passes through it and induces a voltage which can be measured by the spectrum analyzer. This probe requires performing the measurement in different orientations to capture each magnetic flux components. Probes frequency range is given by the manufacturer for both Electric and magnetic field probes.

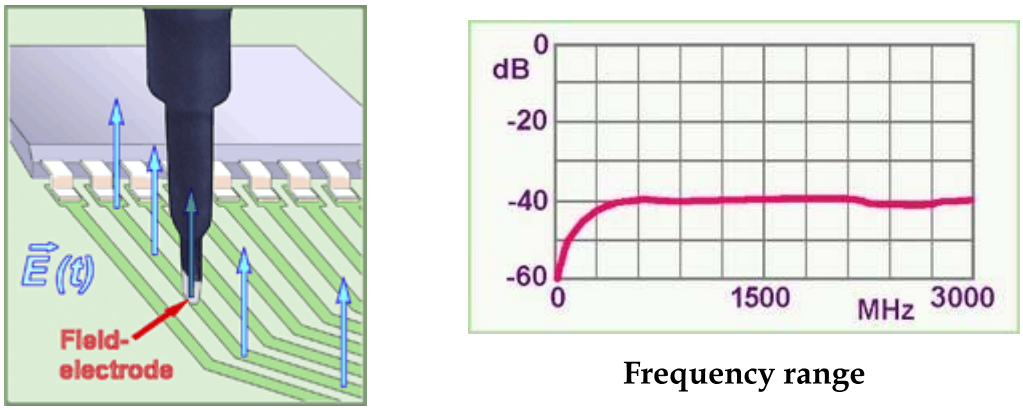


Figure 76: Langer Electric field probe [39]

The electric field probe measures the vertical component of the electric field. The capacitive coupling between the coaxial core and the device under measurement induce a current which can be measured via the input impedance of the analyzer.

Only Magnetic field probe will be used because it decreases disturbances due to common mode variations. By this way the power network can be excited in common mode whereas the magnetic field is measured. The

spatial accuracy of the probe does not allows to distinguish resonance localization under bonding wire size (spatial resolution about 1mm). Magnetic probes can measure the magnetic field for several orientations. The Figure 77 gives the orientation nomenclature convention which will be used in this document.

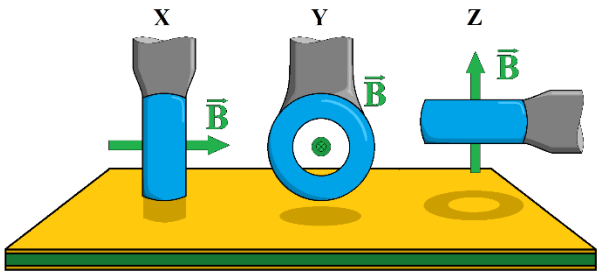


Figure 77: Magnetic field probe orientations

Sweeping all frequencies with the near field measurement bench takes a lot of time. However in combination with the global resonance analysis measurement, it is possible to perform near field measurement only at global resonance frequencies to determine resonance locations.

Measurement bench validation with a simple circuit

To validate the measurement method, a test was performed on a 3cm wires as illustrated in Figure 78. The global resonance analysis provides a resonance frequency of 70MHz. The near field measurement was performed at this frequency and gives results depicted in Figure 79 with the magnetic field probe for x and y orientations.

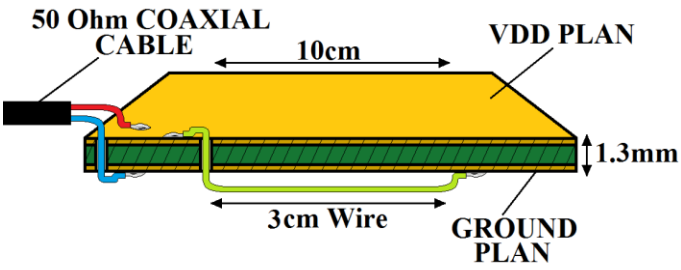
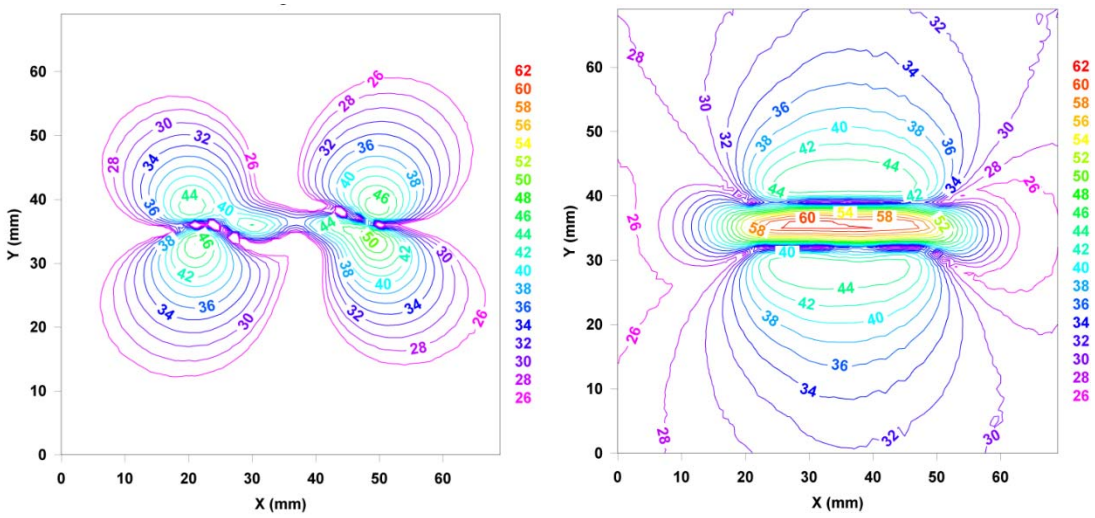


Figure 78: 3cm simple wire board schematic



x orientation **y orientation**

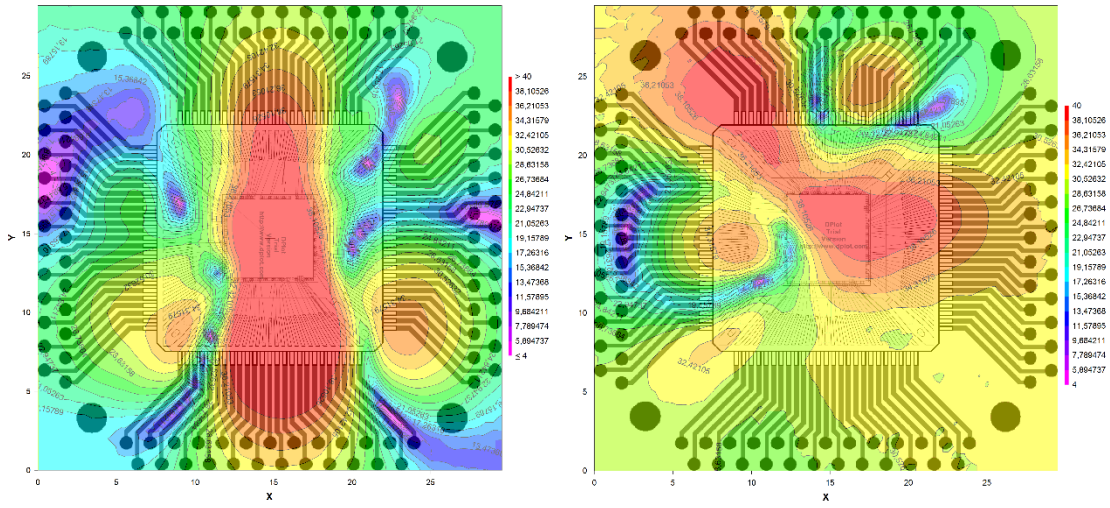
Figure 79: Simple wire near field measurement at its resonance frequency amplitude

The resonant wire is clearly identifiable in the y orientation measurement result because its localization corresponds to the maximum amplitude measured magnetic field. Field amplitude peaks, observables in the x orientation graph (cf. Figure 79), are due to the side effect caused by the wire curve for the board connection.

Microcontroller measurement

This methodology is now applied on a microcontroller. As explained before, the spatial accuracy of the near field probe allows to localize resonances on bonding wires but not in the die. Usually microcontrollers are supplied by several bonding wires distributed around the chip. To localize a resonating bonding wire gives enough information on the sensitive area. A measurement result example on a QFP100 package is depicted in Figure 80.

The example corresponds to the same microcontroller which is measured in the conducted emission method explanation in Figure 72. The analysis frequency at 630MHz has been chosen according to the conducted emission local analysis results. This frequency is deliberately high to clearly see local resonance in the graph. Indeed the lower is the frequency the more homogeneous is the power network in term of amplitude.



x orientation **y orientation**

Figure 80: Near field measurement result at 630 MHz

Only relative amplitude between different areas of the power network is interesting. The x orientation measures the horizontal magnetic field component with respect to the Figure 80 and the y orientation the vertical magnetic field component. It means that the red area visible in the x orientation corresponds to resonating vertical wires or wire with a vertical component. For example a resonating wire located in a corner which is oriented at 45° emits a magnetic field visible at 50% in the x orientation and 50% in the y orientation.

As explained before the spatial resolution of the near field probe permits to see the field generated by the PCB and wire bonding, but does not allow to distinguish resonating routing at the silicon level.

This method allows the identification of resonating area without modifying the power network. It provides important information for investigation purpose. Indeed if a susceptible IP is close to a resonating wire, it has more change to fail, a solution to protect it can be to change the power network resonance location or frequency.

2.4 Investigation methods comparison

This chapter will be concluded by a comparison between all analyses methodologies proposed in this chapter. Each of them has its advantages and

drawbacks depending on the difficulty to set up the bench, the test duration or the accuracy of the analysis.

The first row "bench cost/size/difficulty" gives a global appreciation of the financial investment needed to perform the analysis for a basic EMC laboratory. The analysis duration corresponds to the time necessary to perform the analysis which goes from few second to several hours or days. The special accuracy determines the capacity of the bench to distinguish spatial resonance area. The Usual EMC material topic shows if the analysis is possible with tools available in a basic EMC laboratory or if a specific tools needs to be created or bought. The "Specific board" topic does the distinction between analysis which needs a specific board, the same board as the FTB test board or if any board is compliant.

Global Resonance analysis

Analysis characteristic	☺	😐	☹
- Bench cost/size/difficulty	x		
- Analysis duration	x		
- Spatial accuracy			x
- Usual EMC material	x		
- Specific board		x	

The global resonance analysis bench is a quick approach which provides information for the first investigation step. This measurement is very easy to put in place in an EMC laboratory (Only TEM Cell and signal generator and spectrum analyzer needed) and is very fast (about 20 seconds). This analysis is declined into two complementary variant, the common mode and the differential mode one. In all cases, this is the first analysis to perform as it provides useful information to set other methods. Nevertheless the spatial accuracy is inexistent because it is a global analysis. It uses a specific board but the same as all other emission tests. So if there is some EMS problem other investigation methods are mandatory.

Conducted emission

Analysis characteristic	☺	😐	☹
- Bench cost/size/difficulty		x	
- Analysis duration		x	
- Spatial accuracy		x	
- Usual EMC material	x		
- Specific board			x

The advantage of the conducted emission measurement compared to other methods is that the result doesn't depend on the coupling factor between electromagnetic field and measurement tool. It is the only one proposed which doesn't use electromagnetic field as observation mean. The main drawback is that it requires the design of a specific board which can be expensive. Each spatial point must be measured one after the other and make the analysis duration very long (more than 1 hour for 50 measurement points) and requires lot of handling. The spatial accuracy is limited to connected IOs. Only a spectrum analyzer and a signal generator, which are current tools in EMC lab, are needed. Notice that by this way, observing the supply network modify its behavior. It is something which needs to be kept in mind when applying this analysis method.

Near field measurement

Analysis characteristic	☺	😐	☹
- Bench cost/size/difficulty			x
- Analysis duration			x
- Spatial accuracy	x		
- Usual EMC material			x
- Specific board	x		

The near field measurement bench allows to pass quickly to a second step of investigation if the laboratory is equipped with a near field measurement bench. Indeed no specific board is required, the same as the global resonance analysis method can be used. The spatial sweep is very long (approximately 20

measurement point per minute) but if the global resonance analysis is performed before, only resonances frequencies need to be analyzed. The special accuracy depends on the sweeping steps and the near field probe. An accuracy about 1mm can be expected. This method uses a material non usual in EMC labs, indeed a near field scan bench in required.

3 In silicon analysis

A solution by a direct observation of the supply inside the chip has also been studied during this thesis work. Methodologies proposed before, use the radiated electromagnetic field or an IO to observe the supply network. In this part the possibility to observe directly the supply inside the chip is studied.

As explained before, micro probing is not conceivable in the FTB case because of coupling between stress and cables. The idea of the presented solution is to reduce at its maximum the coupling between the measurement circuit and the stress generator by decreasing its size. A measurement circuit embedded in the microcontroller fulfills this need.

According to constraints explained above, a circuit was developed and put in a test chip to perform measurements during a stress. This circuit presented in Figure 81 resulted in a patent [40].

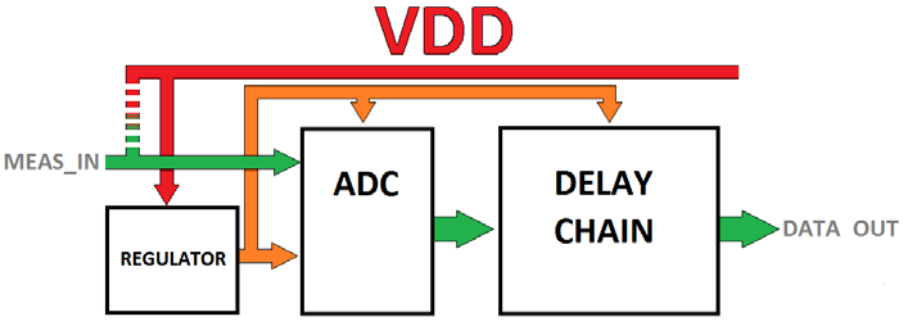


Figure 81: Internal measurement circuit principle

The principle of this architecture is to measure the supply (or any other signal) during the stress with an analog to digital converter. The conversion permits to increase the robustness of data to supply variation. A delay is added between the ADC and the pad in order to collect information on pins by external

tools after the EFT stress, with a clean electromagnetic environment. The delay may be longer than the EFT stress.

To have a circuit which function correctly during the stress, its supply must be protected against it. For this purpose, diodes are used to clamp the regulated voltage to a maximum value like illustrated in Figure 82. This method is used in order to have a relatively stable voltage even for fast variations of the supply. The regulator voltage is tunable by changing the number of diodes.

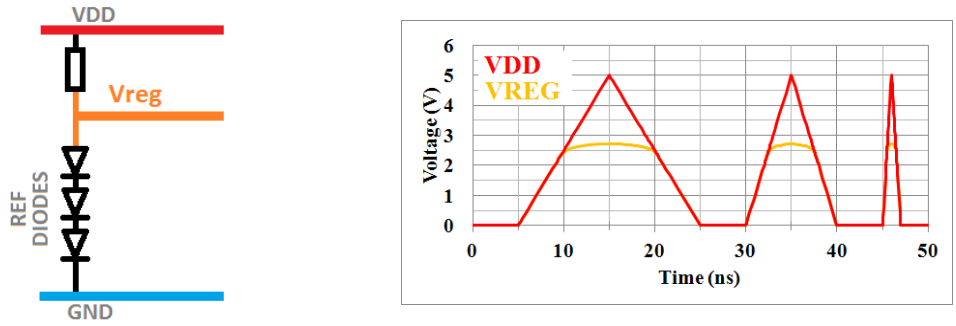


Figure 82: Diode regulator principle

The ADC flash based architecture [41] is used for its speed. Its accuracy is tunable by changing the number of resistances in the voltage divider. It is a very fast ADC because all bits are computed in parallel, there no conversion time window. This ADC Flash architecture uses the diodes regulator to be robust to supply variations, as shown in Figure 83.

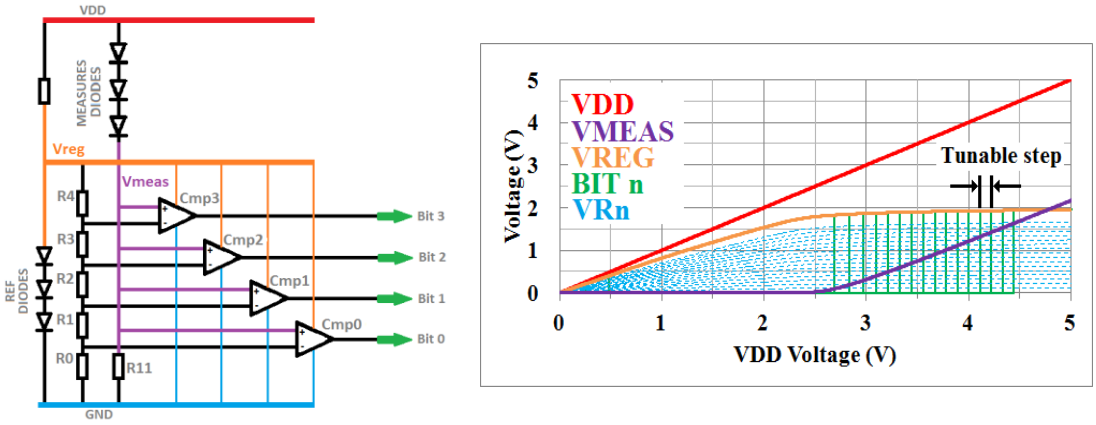


Figure 83: ADC Flash and regulator schematic and simulation

"Measures diodes" are added in order to start the voltage measurement window "Vmeas" when the regulator voltage is stable (cf. Figure 83). The measurement window is defined by the number of diodes.

Simulation of the architecture gives satisfactory results as it can be seen in Figure 84. The reaction delay of the ADC can be observed in the simulation but it doesn't distort measurement. Indeed, each bit state changes when the supply voltage pass its threshold.

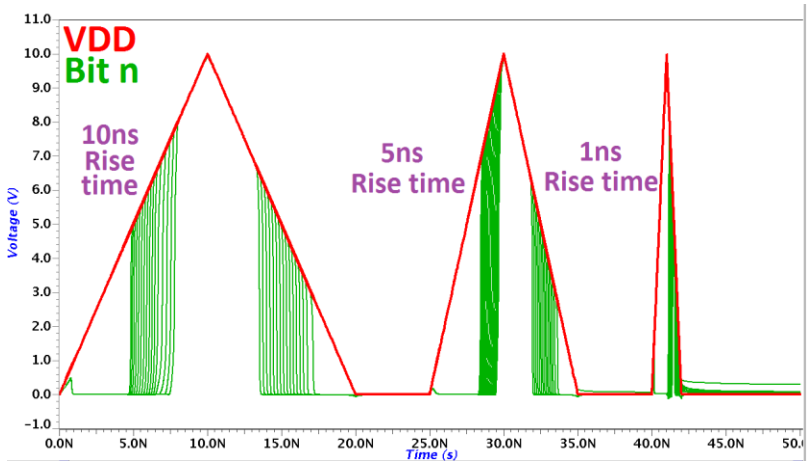


Figure 84: ADC dynamic behavior

Bits generated by the ADC are propagated thanks to delay cell to output pins. Delay cells must take into account the skew to keep the signal integrity from the ADC to outputs. The chosen delay cell based on level shifter architecture [42] is represented in Figure 85. This cell propagates as well the bit and its complement. By this way, the data is propagated without too much degradation through cascaded delay cells.

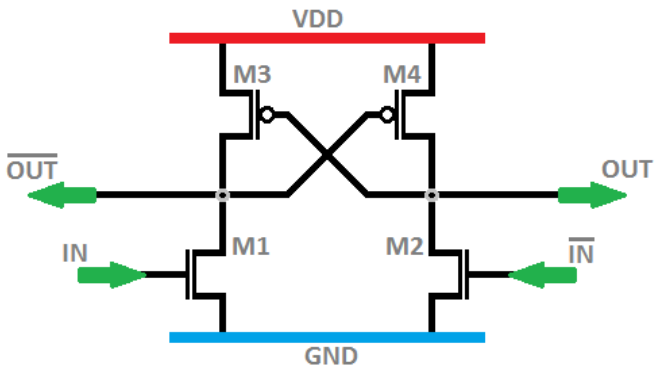


Figure 85: Level shifter based architecture schematic

The simulation result, given in Figure 86, shows how bits are propagated trough 50 and 100 delay cells that is to say more than 50ns delay when the circuit is supplied at 3.3V. A delay difference appears between the ADC measurement and the output data because of the supply variation during the stress. However the amplitude information is not degraded.

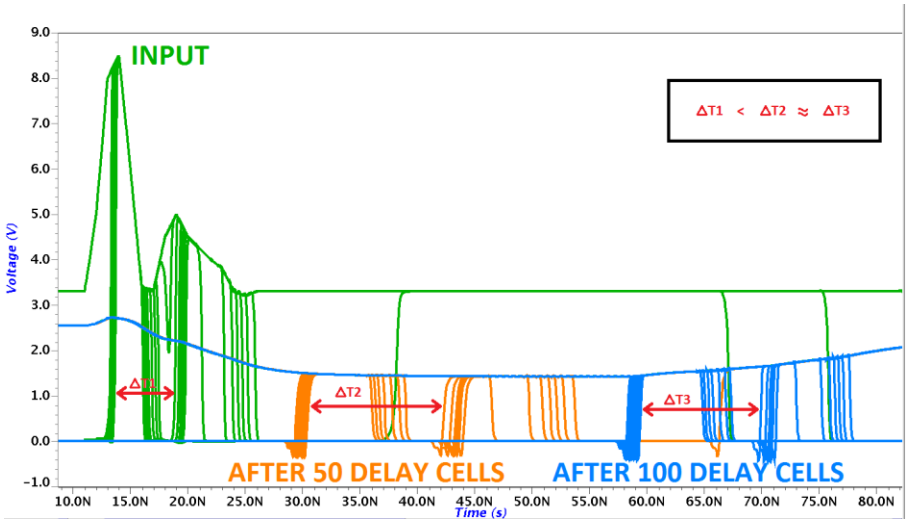


Figure 86: Level shifter based architecture skew

A 16 bit resolution of this circuit was implemented in a test chip. The layout of the circuit alone is represented in Figure 87 and its implementation with IOs in Figure 88.

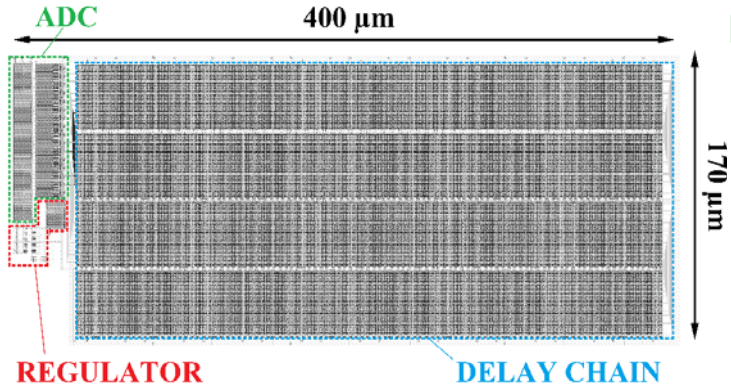


Figure 87: Circuit layout alone

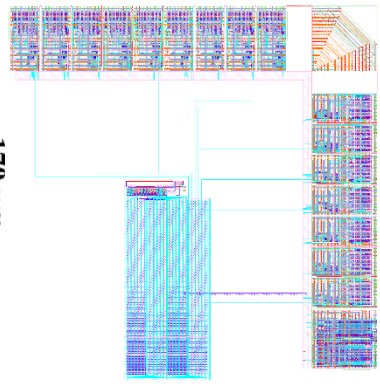


Figure 88: Test chip layout

The measurement window of this test chip is tuned from 2.5V to 4.7V by adjusting the number of regulator and measure diodes. A low frequency measurement permits to validate the correct behavior of the circuit. The Figure

89 shows the measurement result for 3 bits among the 16. Bits state change correctly when their threshold is reached.

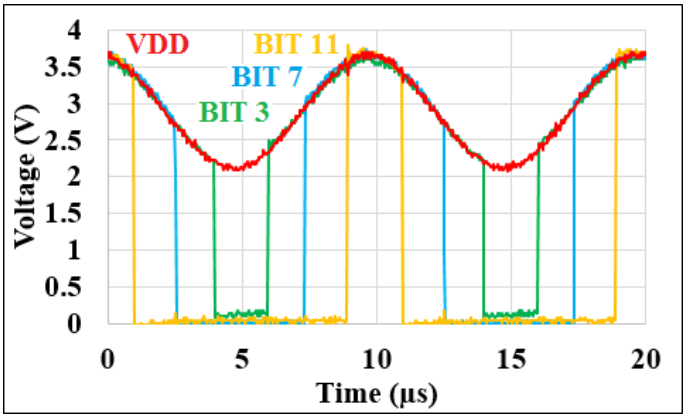


Figure 89: Test chip low frequency measurement (100 kHz)

In this thesis work, the in silicon measurement approach was abandoned in favor of non-invasive methods studied in the beginning of this chapter. Indeed integrating this kind of sub circuit in a microcontroller supposes an additional area and does not permit the analysis of existing products. Therefore, the priority was put on free analysis in term of manufacturing cost.

However, obtained results are encouraging and a deeper study and improvement of such circuit could provide a powerful tool for microcontroller failure analysis.

4 Conclusion

When a microcontroller fails to the FTB test, nowadays, no measurement is possible during the stress to help investigation. The supply network has a huge influence on test results. Indeed, the stress applied in common mode on supply is transformed into differential mode inside the chip due to dissymmetry between power and ground path. It was seen that parasitic elements of power network constitute a passive and potentially resonant circuit. Characterizing the supply network gives significant information on the stress propagation mechanisms.

Usual measurement methods are not applicable easily as the output of the supply network is inside the chip. Resonances were identified as potential weakness for the device under test. In this sense, three analysis methods were developed to identify resonance frequencies using indirect measurement. The global resonance analysis method uses the electromagnetic field emitted by the supply network when it is excited by a perfect sinusoid to characterize its frequency response. This tool gives an overview of weak frequencies of the device. But it was also seen that resonance can be spatially localized inside the die. Two analysis methods were developed in this direction. The first one is the conducted emission analysis method which uses the conducted noise emitted by the power network through IOs when a perfect sinusoid is applied on it. And the second one is very close to the global resonance analysis method but uses a near field probe to measure the electromagnetic field at any point above the circuit. By this way peak emission point can be localized. Finally, a fourth method using a measurement circuit in silicon was approached. Its principle is to measure the internal supply voltage thanks to a fast robust ADC. Abandoned for this work in favor of less silicon surface cost methods, this can be a good way to follow for future work.

Three tools helping investigation on fails at FTB test were provided in this chapter. This will help fail debug and chip robustness improvement. The next chapter will deal with a global debug methodology using those tools on a real case. It will also show how it is possible to improve microcontroller robustness by playing on power network resonance frequencies.

Chapter 4 Robustness improvement application & perspectives

The problematic leading to this study is that nowadays, there is no investigation tool able to debug a microcontroller which fails to the FTB test. The test bench was introduced and first measurements shown that the power network has a huge impact on FTB test results. Propagation mechanism was studied and it was shown that the common mode to differential mode conversion is the cause of device fails. This conversion has maximum amplitude when a power network resonance occurs. Investigation tools showing those resonance phenomena were developed.

To demonstrate the interest of tools presented in the previous chapter, and show how they help to improve microcontroller robustness, the focus will be put on external parameters from the chip itself. Through several study cases, the contribution and new investigation perspectives provided by those tools will be highlighted. It will be shown that a microcontroller can be improved in term of robustness without modifying the silicon.

1 Acting on external parameters modify robustness threshold

It was previously demonstrated that FTB fails come from common mode to differential mode conversion due to dissymmetry between VDD and VSS paths. The dissymmetry between VDD and VSS are mainly caused by parasitic RLC of the power network. In the Chapter 2 most influencing parameters are described. The silicon contains potentially weak circuits, but it was seen that a lot of influential parameters on common mode to differential

mode conversion are external to the silicon itself. Indeed test bench, PCB and package has a significant contribution on the power network dissymmetry. As microcontroller manufacturer, we can't act on test bench parameters since it is a standard. It is obviously possible to correct on silicon but this option is very expensive. Thereby, the focus will be put on package setup or connection to PCB and there influence on FTB test results. This way could also help to provide guidelines to customers.

1.1 Which external parameters

Whereas a silicon modification is very expensive, external parameters can be modified more easily. Indeed as well for experimentation or manufacturing, it is possible to modify the PCB routing or the bonding diagram to change the common mode to differential mode conversion of the FTB stress. This allows to create several variations of the same chip.

1.1.1 Package

The package is the external element the closest to the chip. It contains influencing parameters in common mode to differential mode conversion since supply bonding wires are most of the time non symmetric. So one of the preferential parameters to modify in package is the numbers of supply and ground pins, bonding wires and their position.

The package contains also a die pad which will be described later in this part. It is suspected to be also a contributor to the common mode to differential mode conversion as it is in the VSS path.

1.1.1.1 Supply and ground bonding diagram

In microcontrollers, several supply pads are available all around the chip, allowing several supply bonding setups. This particularity will be used to modify the supply network and so the way in which the stress is transformed. This modification is made by changing the bonding diagram of the package.

1.1.1.2 Die pad connection

In previous chapter, it was shown that FTB issues are due to the transformation of the stress from common mode to differential mode. This transformation is due to dissymmetry between VDD and VSS path between the stress injection point and the circuit inside the chip. Regarding to a microcontroller package, the die pad could be a significant dissymmetry contributor. The die pad is a metal plane on which is pasted the silicon inside the package as illustrated in Figure 90. It is connected to the ground thanks to VSS bonding wires from pin to the die pad. It is used to connect VSS pad on it without using external pins.

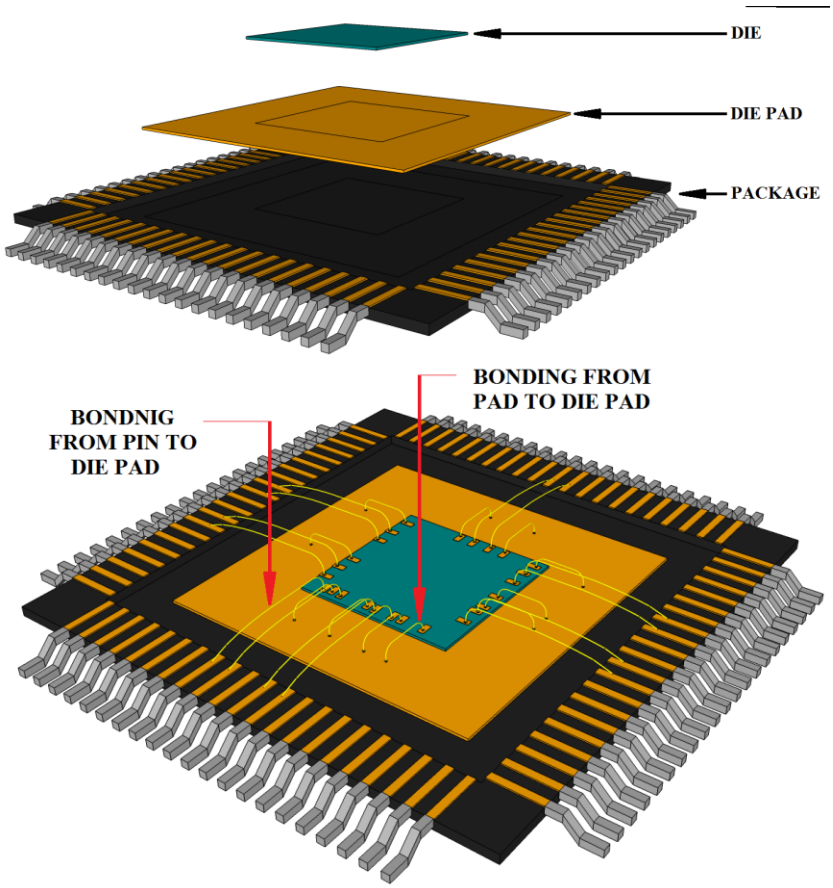


Figure 90: Die pad in QFP100 package

1.1.2 PCB supply tracks

In test conditions, the chip is in a package which is welded on a PCB. Supply routing which leads to package pins is on the PCB. Modifying the PCB allows to change the supply network. Moreover, it was seen previously that the

PCB supply routing is also a big contributor in common mode to differential mode conversion. In this chapter PCB supply and ground tracks will be cut or not, allowing to make several variants of supply network for the same microcontroller. This method offers the advantage to be cheap, and can offer a great help if it permits to solve FTB issues.

2 Die pad effect study

This part is dedicated to the study of the effect of the die pad on robustness. In order to achieve this study, two microcontrollers in two different packages, but with several bonding diagrams will be used. For confidential purpose, they will not be named with their official names. Those microcontrollers will be called CHIP 1 and CHIP 2. Names are used to identify the silicon chip only independently to the assembly.

Microcontrollers used for this study are both from STM32F4 family. They are a 32 bit microcontroller made in 90nm technology node. They embed an ARM Cortex M4 core. As shown in Figure 91, they are a High performance microcontroller which can be used for many kinds of applications.

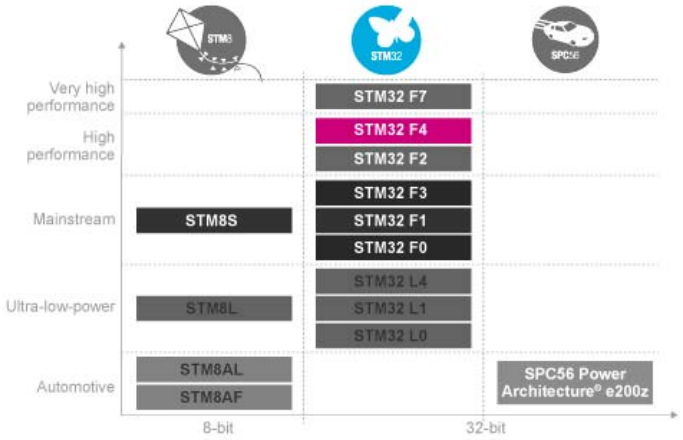


Figure 91: STM32 F4 in all ST microcontroller families

The package used for this study is a QFP100 for CHIP 1 and QFP144 for CHIP 2. Those microcontrollers were both assembled with and without die pad. The die pad is disconnected by removing in the bonding diagram all wires

coming from pin to the die pad and from die pad to pad on silicon. By this way, the die pad is totally independent from the power network.

2.1 Die pad contradictory influence

The two microcontrollers chosen for this study are different but quite similar. Both CHIP 1 and CHIP 2 are from the same platform. It mean that they contain the same IPs, they are made with the same flow in the same technology. Moreover, respectively, all CHIP 1 and CHIP 2 in the various assembly are from the same wafer. All this parameters make the two study cases very close each other.

2.1.1 CHIP 1

The two versions of the CHIP 1, with and without die pad, have robustness thresholds summarized in Table 16.

Table 16: CHIP 1 FTB results with and without die pad

Die pad	FTB_{th+}	FTB_{th-}
with	3.0kV	-2.9kV
without	2.0kV	-1.6kV

The CHIP 1 with the die pad is more robust than without die pad. Adding a die pad seems to improve the chip robustness. If it is true for all packages it could be a simple way to enhance FTB results without modifying the silicon. Let's see the results of the CHIP 2.

2.1.2 CHIP 2

The Table 17 shows the robustness threshold of the CHIP 2 with and without die pad.

Table 17: CHIP 2 FTB results with and without die pad

Die pad	FTB_{th+}	FTB_{th-}
with	0.8kV	-0.8kV
without	1.4kV	-1.3kV

For the CHIP 2 the result is completely different, adding a ground die pad degrades FTB robustness. Which mechanism creates this kind of difference? Of course, the die pad is a significant part of the power network, but this one is too complex to anticipate such result.

2.1.2.1 Die pad conclusion

The influence of the die pad was studied with the help of two different but similar microcontrollers CHIP 1 and CHIP 2. The result obtained with the simple FTB test does not permits to conclude on any reproducible effect of the die pad between different products, even when very similar in the same design, process and platform. But anyway, results show that the die pad have clearly an influence on robustness to FTB test. Without better understanding of FTB stress, the influence of the die pad would not be understood and its usage for robustness improvement would probably be considered as impossible. It was the situation before this thesis work.

2.2 How resonance tool helps to give coherence

In the previous section the study is only based on package modification and FTB tests. The FTB test alone shows contradictory results regarding the die pad and doesn't permit to conclude on exploitable result. Let's see what happens in term of resonance frequencies using the differential global resonance analysis method presented in the previous chapter.

2.2.1 CHIP 1

The global differential mode resonance analysis presented in the Chapter 3 is applied on both setup of the CHIP 1. The measured resonance spectrum is depicted in Figure 92. For clarity purpose only one orientation, which contains the same resonance frequency value than the other, is represented in the graph.

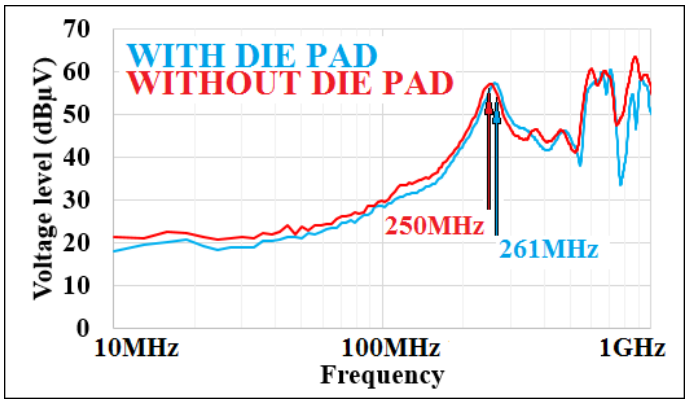


Figure 92: CHIP 1 die pad influence on resonance

The amplitude of these spectrums is not relevant because it depends on several parameters such as the power distribution network (number and location of pins), the package, the die pad, … Those parameters modify the coupling factor between the DUT and the TEM cell. So we only consider the value of the resonance frequencies. The influence of the die pad results in a shift of the first resonance frequency about 10MHz (from 250 to 261 MHz). Thanks to this result, it is difficult to correlate this low difference (between these two spectrums, 10 MHz shift) with the FTB measurements (more than 1 kV with and without the die pad). However, we continue to explore this method in order to investigate the FTB measurement discrepancy on the two chip versions.

2.2.2 CHIP 2

The CHIP 2 is in a QFP144 package. In such package, parasitic elements have higher values than in QFP100. As a consequence resonance frequencies should be lower. The Figure 93 shows the resonance frequency spectrum of the CHIP 2 with and without die pad.

As for the CHIP 1, the die pad has the same effect in term of resonance frequency, which shifts from 68MHz to 86MHz, but the effect is opposite on the FTB robustness (cf. Tables 16 and 17).

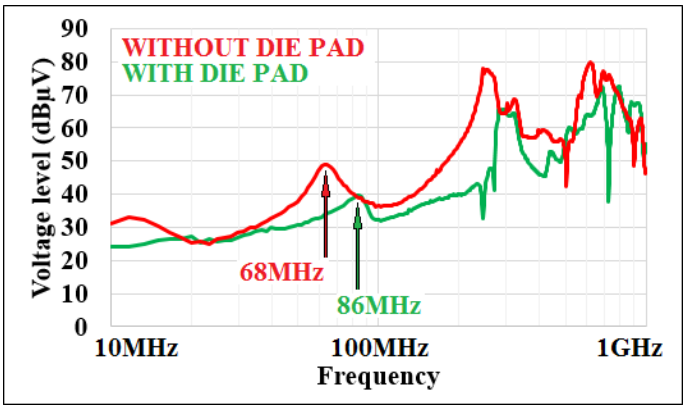


Figure 93: CHIP 2 die pad influence on resonance

2.3 Conclusion

The die pad is an element inside the package which influences clearly FTB test results. Its effect on the two test cases does not go in the same way. It improves performances of the CHIP 1 whereas it degrades the FTB robustness of the CHIP 2. But, the global resonance analysis tool gives coherence to the effect of the die pad (high resonance frequency shift). So, it is difficult to conclude about the FTB resonance with only a global resonance analysis using a TEM cell. Indeed, using this analysis method, we have no information about local resonance frequencies and supply pins weakness. We have shown in chapter 2, that the number of supply pins and their locations have great influence on the FTB robustness. So what is the correlation between the number of supply pins and the resonance frequencies?

3 Using resonance tool to determine a weakness zone

Results of the die pad influence study lead to imagine a weak zone. Indeed the two different chips have not the same reaction to the resonance frequency shift. This behavior happens for the die pad but is it valid if the resonance frequency is shifted with another way? In this section several means to shift resonance frequency will be tested for CHIP 1 and CHIP 2, and

resonance frequency spectrum will be put in front of FTB test results to understand microcontroller's behavior.

3.1 Resonance frequency shift using PCB and package on CHIP 2

In addition of the die pad influence study, we will modify the connection on the PCB of CHIP2. In Figure 94, we consider 3 cases:

- Case 1 : QFP144 with die pad (same as Figure 93)
- Case 2 : QFP144 with die pad and with PCB modification (all VSS tracks connected to the die pad are cut)
- Case 3 : QFP144 without die pad (same as Figure 93).

Regarding those resonance spectrums it seems that the more the resonance frequency increases, the more the chip is susceptible. To complete this information, the CHIP 2 was assembled in a QFP100 package to shift the resonance frequency higher.

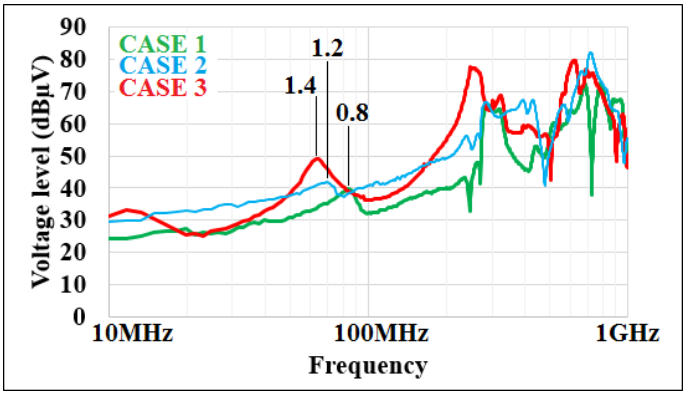


Figure 94: CHIP 2 Resonance spectrum and FTB robustness threshold

Two versions of the QFP100 with and without die pad were tested and measured thanks to the differential global resonance tool. The Figure 95 gives the resonance spectrum and the Table 18 summarizes FTB test results.

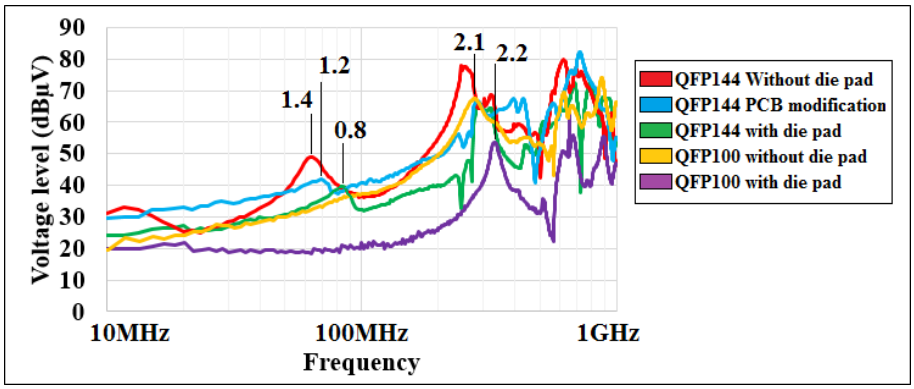


Figure 95: CHIP 2 QFP144 and QFP100 Resonance spectrum and FTB robustness threshold

Table 18: CHIP 2 Resonance frequency shift and FTB robustness threshold summary

Version	FTB_{th+}	FTB_{th-}
QFP144 With die pad	0.8kV	-0.8kV
QFP144 PCB modification	1.2kV	-1.0kV
QFP144 Without die pad	1.4kV	-1.3kV
QFP100 Without die pad	2.1kV	-1.1kV
QFP100 With die pad	2.2kV	-1.1kV

As expected the QFP100 package has higher resonance frequency than the QFP144 and the chip is more robust against FTB aggressions. Moreover, the addition of the die pad increases again the resonance frequency. This analyze highlights a frequency weak zone estimated around 150MHz. Indeed the robustness decreases when the first resonance frequency comes close to this value. In order to finish this study, we want to show if we have the same behavior with CHIP1 mounted in a QFP100.

3.2 Resonance frequency shift of CHIP 1 by supply bonding diagram change

The same method will be used for the CHIP 1. The microcontroller was assembled with several bonding diagrams chosen arbitrarily. As usual, all CHIP 1 are from the same wafer. Those bonding diagrams play with the number of supply couple, but also with the number of VDD and VSS bonding wires

independently. The Figure 96 shows differential global resonance analysis of different assembly version and their positive robustness threshold in kV, written over the resonance frequency peak.

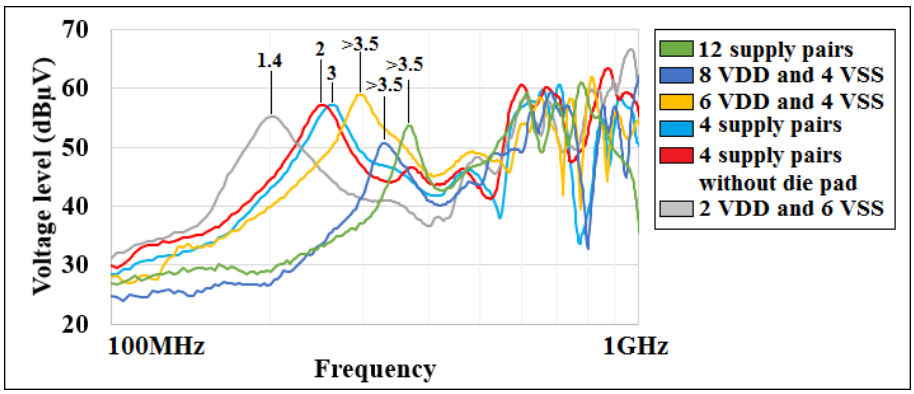


Figure 96: CHIP 1 Resonance spectrum t and FTB robustness threshold

Those resonance frequency spectrums put in front of FTB robustness threshold suggest a weak zone. Indeed for the CHIP 1 the less is the resonance frequency, the less robust is the microcontroller. As for CHIP2 using a QFP100 package, the circuit is more robust with the die pad.

3.3 Conclusion

Several versions of the same chip were tested and have different robustness levels. Comparisons between different FTB tests are very difficult to interpret. Thanks to resonance analysis developed in the Chapter 3 the coherence of chip behavior was understood. Moreover, those tools permitted to determine a frequency weak zone where a resonance makes the chip more susceptible. The advantage of tools developed during this work was demonstrated but their potential is far to be completely exploited.

4 Perspectives

This thesis work permitted to understand FTB disturbance propagation mechanisms. This comprehension leads to the creation of power network analysis tools based on resonances. The usage and interest of one of those tool,

using the same principle than all others, was demonstrated for concrete cases in this chapter. Because a thesis work needs to be closed one day, the time is missing to develop others. This part will give a preview of what could be the next step.

4.1 Using other tools

The interest of the global differential resonance analysis was demonstrated in this chapter. It was shown that such tool allows to understand more deeply the impact of a power network modification on its frequency response. It was also shown that this frequency behavior is directly linked to the robustness of the chip when this one contains a weakness.

During this thesis work, 3 other tools were developed based on the same principle: the Common mode global resonance analysis, the conducted emission and near field measurement. Another method was studied using an embedded measurement circuit. The interest of those tools was not demonstrated in concrete case. Their principle, based on the same as the global differential mode resonance analysis, described in the Chapter 3 allows to understand that they can provide a great help in the FTB understanding and so to chip robustness improvement.

So, to continue this work using other tools could help to find other way to improve microcontroller robustness. It provides lot of perspectives to continue this work.

4.1.1 Debug flow and directives

All tools developed in this work could be used to be complemental in a debug flow when a weakness is observed. Indeed, using global and local analysis could provide enough information to find a patch allowing to improve the robustness of a microcontroller by using external parameters. By this way FTB issue could be corrected with low cost solutions. It could also be used to provide guidelines to customers for their PCB design in order to avoid FTB issues.

4.2 How to shift resonance at wanted frequency

The first part of this chapter shows that microcontroller can have a weak zone where a resonance frequency of the power network can cause robustness degradation. It was also seen that a modification of parameters of the supply network can change its resonance frequency. But the impact of the power network modification on its resonances is not well understood. Indeed, even if it is possible to anticipate the direction of a frequency shift in some cases, it is difficult to really know its value.

Having a reproductive flow to determine the weak zone and knowing how to change the resonance frequency where it is wanted could be a great help for quick and reliable robustness improvement. Moreover, thanks to this thesis work, lot of influencing parameters on resonance frequency are already known such as die pad, supply and ground bonding and PCB modification. It is also conceivable to add nonfunctional part in a power network such bonding wire inside the package from pad to pad in the power network in order to change resonance frequency.

4.3 Modeling

Simulation could be a great help to predict FTB issues before manufacturing and allows silicon manufacturer to correct dysfunction before the die manufacturing. As a consequence, those predictions permit to avoid the money loss due to a redesign for correction. But simulations need an adapted model to be performed.

Now that FTB stress mechanisms are understood, the creation of models can be conceivable. But the modeling of such phenomena is complex. Indeed several things must be taken in account. The modeling of the stress itself, of the power network behavior, its frequency and transient response and the behavior of potential weak circuit inside the chip are necessary to determine the chip robustness as it is suggested for ICIM modeling method. Such model is

very complex to establish. But some part could be modeled independently and could provide enough information to help chip improvement.

Modeling only the power network could be a first step which allows to understand the effect of its modification on resonances. This imply to model the PCB, the package and the silicon. By this way it is possible to provide to the designer a stress model to simulate their circuits. Another issue with that in concrete situation is that, a chip manufacturer is able to change the chip and the package but the PCB design is in the hands of customers. A good understanding of the power network behavior when it is submitted to common mode disturbance such as FTB stress could permit silicon designers to give directive to customer about the PCB design.

General conclusion

Starting from a very poor set of investigation tools regarding microcontrollers' FTB fails, this thesis work gives keys to understand and analyze FTB failures. No measurement is possible during the FTB stress because the stress itself disturbs measurement tools, and the stress propagation mechanisms are not intuitive. Indeed, the common mode stress introduced by the FTB generator seems inoffensive when applied on both reference and supply nodes. Experimentations using the same chip with several supply distribution network setups show that such modification is able to completely change the FTB test results. By going farther, we showed that the common mode disturbance is transformed into a differential mode stress by the power distribution network. Indeed, parasitic passive elements such as resistance inductance and capacitance, introduce a dissymmetry between the reference and the supply node. Their effects, negligible at low frequency, become significant when the frequency increases. We showed that the order of magnitudes of parasitic elements of the microcontroller's power network in the FTB test condition allows the FTB stress to significantly disturb the microcontroller.

Based on those observations, we developed power distribution analysis methods. A solution using a measurement circuit on silicon was designed, but finally, we focused on less restrictive noninvasive methods. Considering that the power network is a complex RLC structure. Such structure is able to produce resonance phenomena. Those phenomena amplify the common mode to differential mode conversion at resonance frequencies. This particularity was used to develop three power distribution network analysis methods. Indeed, those methods use the electromagnetic emission of the power network to extract its resonance spectrum. Among developed analysis methods, one allows to extract a global resonance spectrum and others to localize resonance area.

In the last chapter, we showed, with the global resonance spectrum, that the resonance frequency of a power network can be modified by any change in it. This phenomenon was used to identify a frequency weak zone of a microcontroller. By this way it was shown that it is possible to make a microcontroller more robust without modifying the silicon. Indeed, a simple modification of the package or PCB is able to improve the robustness.

It is only an example of the contribution of this thesis work usage. This work opens also a lot of perspectives in term of debug, robustness improvement, modeling and simulations.

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Appendix A : Résumé en français

Introduction

Ce travail de thèse a été réalisé au sein de l'entreprise STMicroelectronics à Rousset dans la division microcontrôleurs et plus spécifiquement dans l'équipe en charge de la conception des entrées/sorties. Il a également été effectué en collaboration avec le laboratoire EpOC de l'Université Nice Sophia Antipolis, et financé par l'ANRT.

Dans l'équipe, une thèse traitant de l'émission électromagnétique a déjà été achevée, aboutissant à un modèle réutilisable permettant de prévoir le comportement en émission des microcontrôleurs. Dans une même dynamique d'amélioration constante, ce travail de thèse est consacré à l'étude de la susceptibilité électromagnétique.

L'état de l'art est riche de travaux sur les décharges électrostatiques pendant les phases de manipulation et de fabrication des puces. Ils ont abouti à la conception de protections efficaces. Cependant, une décharge électrostatique ou plus généralement un transitoire rapide peut survenir tout au long de la vie d'un microcontrôleur. Alors que les protections contre les décharges électrostatiques ont encore un effet lorsque le microcontrôleur est en fonctionnement, elles ne peuvent pas protéger des perturbations sur l'alimentation telles que celles définies dans la norme IEC 61000-4-4 [4] traitant des transitoires rapides en salve. Cette norme fait pourtant référence dans l'évaluation des produits.

Les microcontrôleurs sont composés de plusieurs sous circuits qui peuvent être susceptibles aux transitoires rapides sur leur alimentation. Des différences de résultats aux tests ont été observées selon la manière dont sont implémentés (PCB, boîtier …) ces sous circuits. Ce travail de thèse est dédié à la

compréhension de tels phénomènes. Pour cela, ce manuscrit s'organise en quatre parties.

Un premier chapitre sera dédié à la présentation des microcontrôleurs et à leurs applications, afin de définir la problématique et présenter l'état de l'art sur le sujet. Le mécanisme de propagation du stress sera expliqué dans un second chapitre. La compréhension des mécanismes de propagation a permis de développer des méthodes d'analyse des réseaux d'alimentation, qui seront présentées dans le chapitre 3. Puis dans un dernier chapitre, nous allons exploiter les éléments développés dans ce travail de thèse, afin d'améliorer la robustesse des microcontrôleurs.

Chapitre 1 Introduction à la problématique et état de l'art

1 Microcontrôleur

Les microcontrôleurs sont des systèmes qui intègrent tous les éléments d'un micro-ordinateur sur un même circuit intégré. Ils contiennent un microprocesseur qui est le cœur du système, une ou plusieurs mémoires vives et mortes, des circuits analogiques ainsi qu'un grand nombre d'entrées/sorties. Ces systèmes sont programmables et polyvalents. Ils sont donc utilisés dans de très nombreuses applications électroniques, dans tous les domaines.

Dans ce travail de thèse, les microcontrôleurs ST de la famille STM32FX sont spécifiquement étudiés. Ils s'adressent à des applications très variées allant de l'usage général à la haute performance.

Le fait que les microcontrôleurs soient destinés à tout type d'application implique qu'ils soient compatibles avec les exigences de tous les domaines en termes de normes, y compris les plus drastiques.

2 Flot de test électrique des microcontrôleurs

Afin de garantir leur robustesse dans les applications auxquelles ils sont destinés, les microcontrôleurs subissent un flot de tests électriques. Ce flot de tests est divisé en deux parties : en premier lieu, les tests de robustesse physique aux agressions électriques, puis, les tests de compatibilité électromagnétique.

2.1 Tests de robustesse physique

Le flot de tests de robustesse physique comprend les tests de décharges électrostatiques correspondant aux normes HBM (Human body model) et CDM (Chip Discharge Model) ainsi que le test de latchup. Chacun de ces tests est défini par une norme internationale, et met en jeu différents mécanismes de défaillance. Chacun de ces mécanismes est anticipé et protégé par des implémentations et des circuits spécifiques dans le microcontrôleur. Lorsqu'une défaillance est observée, c'est-à-dire que le circuit subit des dommages physiques, le microcontrôleur retourne à l'étape de conception afin de développer un correctif.

Une fois la robustesse physique vérifiée, le microcontrôleur passe par les tests de compatibilité électromagnétique ou CEM. La CEM est la capacité d'un circuit, d'un système ou d'un équipement électrique, à fonctionner de manière satisfaisante dans son environnement électromagnétique, sans introduire de perturbation intolérable pour cet environnement. La compatibilité électromagnétique introduit donc les notions de susceptibilité aux agressions et d'émission de perturbation. Dans le cadre de cette thèse, c'est la notion de susceptibilité qui va être étudiée.

2.2 Compatibilité électromagnétique

De la même manière que pour les tests de robustesse physique, les microcontrôleurs sont soumis à un flot de tests de robustesse aux agressions électromagnétiques. Cette fois-ci, le microcontrôleur exécute un programme.

Une défaillance correspond donc à une mauvaise exécution du programme ou à des dommages. Les microcontrôleurs sont soumis à deux tests de robustesse aux agressions électromagnétiques. Le premier est le test de décharge électrostatique fonctionnel défini par la norme IEC 61000-4-2 [3]. Chaque patte du microcontrôleur subit une décharge positive et négative pouvant aller jusqu'à plusieurs kV d'amplitude. La correcte exécution du programme est vérifiée. Lorsqu'une défaillance est observée, le seuil de tension, auquel elle est survenue, est noté et correspond au seuil de robustesse du microcontrôleur. Si ce seuil est considéré comme trop bas, le microcontrôleur retourne à l'étape de conception de manière à être corrigé.

Le deuxième test de robustesse aux agressions électromagnétiques, celui qui fait l'objet de cette thèse, est le test de transitoires rapides en salve ou FTB (Fast Transient Burst) défini par la norme IEC 61000-4-4 [4].

2.3 Le test de transitoires rapides en salve (FTB)

Dans le cas des microcontrôleurs, le test FTB est appliqué à l'alimentation du circuit. Le microcontrôleur est connecté à son alimentation et exécute un programme représentatif de son fonctionnement normal. Un dispositif, appelé pince de couplage, est ajouté sur les câbles d'alimentation et permet d'y connecter le générateur de perturbation FTB. De cette manière, les perturbations sont appliquées sur l'alimentation du microcontrôleur par couplage capacitif. Ces perturbations sont en mode commun, c'est-à-dire que les fils de masse et d'alimentation reçoivent le même stress. Cette perturbation est appliquée de manière répétitive « en salve » et à une amplitude pouvant atteindre 3.5kV dans notre cas. Les perturbations sont appliquées à des amplitudes croissantes dans les polarités positive et négative. Lorsqu'une défaillance est observée, l'amplitude est notée et correspond au seuil de robustesse du microcontrôleur. Si ce seuil est trop bas, le microcontrôleur retourne à l'étape de conception pour être corrigé.

Pour ce test, le microcontrôleur est placé sur un PCB compatible avec tout le flot de compatibilité électromagnétique, y compris les tests d'émission.

Cette carte correspond au standard IEC 61967-2 [17], avec uniquement deux couches : une couche de signal et alimentation et un plan de masse.

De nos jours, aucune protection spécifique aux perturbations de type FTB n'est implémentée dans les microcontrôleurs. De plus, il est extrêmement difficile de trouver la cause d'une défaillance et donc d'y trouver un correctif. En effet, pendant une perturbation FTB, aucune mesure n'est possible. Le transitoire rapide appliqué au microcontrôleur perturbe également les mesures par couplage électromagnétique.

L'état de l'art est pauvre sur le sujet du test FTB, que ce soit dans ses protections ou dans la compréhension des mécanismes de propagation et défaillance. Des modèles orientés vers la susceptibilité électromagnétique existent, tel que le model ICIM (Integrated Circuit Immunity Model) [22], afin d'effectuer des simulations. Mais comprendre les mécanismes de propagation du stress est essentiel pour élaborer un modèle correcte. Dans ce travail de thèse, nous allons donc essayer de donner les clés pour comprendre les mécanismes de propagation du stress FTB.

3 Conclusion

Les microcontrôleurs sont des systèmes électroniques intégrés destinés à un très grand nombre d'applications dans des domaines très variés. Cette polyvalence implique d'être compatible avec toutes les normes de robustesse aux agressions électriques des marchés visés. Parmi toutes ces normes, ce travail de thèse se focalise sur le test FTB, faisant partie des tests de compatibilité électromagnétique. Afin de comprendre les mécanismes de propagation des perturbations en mode commun du test FTB, ce document va s'articuler en plusieurs parties.

Dans le chapitre suivant, les mécanismes de propagation du stress et des défaillances seront étudiés. La compréhension de ces mécanismes permettra ensuite, dans un troisième chapitre, de développer des outils d'analyse des microcontrôleurs afin de détecter leurs faiblesses. Un dernier chapitre sera

ensuite dédié à l'étude de cas, en utilisant les outils mis en place dans le chapitre 3, et aux perspectives ouvertes par ce travail.

Chapitre 2 Compréhension des mécanismes de propagation du stress FTB

Le stress FTB est appliqué à l'alimentation des microcontrôleurs. Nous allons donc étudier l'impact des modifications du réseau d'alimentation sur les résultats au test FTB. Les microcontrôleurs sont conçus de manière à s'adapter à plusieurs boitiers. Pour cela, un grand nombre de plots (ou pads) d'alimentation sont disponibles tout autour de la puce. Il est donc possible de faire varier le nombre de connexions puce/boitier, ainsi que leurs emplacements. Cette possibilité va être exploitée afin d'étudier l'influence du réseau d'alimentation sur le seuil de robustesse des microcontrôleurs.

1 L'influence du nombre d'alimentations et de leurs emplacements sur les résultats au test FTB

Une puce de la famille STM32F4XX a été utilisée pour cette étude. Le microcontrôleur dispose de 12 couples de pads d'alimentation et de 2 pads destinés à connecter des capacités externes au régulateur intégré. Ce microcontrôleur a été assemblé dans un boitier QFP100 avec différentes configurations. Toutes les versions présentées dans ce chapitre utilisent une puce provenant de la même plaquette silicium.

Les premières versions font varier le nombre de connexions aux capacités externes du régulateur. 4 versions ont été réalisées : avec un ou deux condensateurs externes connectés, et deux variantes du nombre

d'alimentations. Les résultats sont différents selon qu'il y ait une ou deux capacités externes connectées. Le nombre de capacités externes du régulateur a donc une influence sur le seuil de robustesse du microcontrôleur. Dans la suite du document, deux condensateurs externes seront donc systématiquement connectés.

Nous avons mené une deuxième phase de test faisant varier le nombre de couples d'alimentations. Le nombre de masses étant égal au nombre d'alimentations, différentes versions, avec des nombres de couples d'alimentations allant de 2 à 12 ont été testées. Les résultats obtenus laissent penser que plus le nombre de couples d'alimentations est élevé, plus le microcontrôleur est robuste au stress FTB.

Une troisième phase de test avec 4 couples d'alimentations, mais avec différentes variantes de placement de ces alimentations a été effectuée. Quatre versions de placement des alimentations ont été implémentées, et donnent toutes des résultats différents au test FTB. Le nombre de couples d'alimentations à lui seul n'est pas le seul facteur influençant la robustesse. Leur positionnement respectif est également important.

Les résultats obtenus durant cette étude ne permettent pas de conclure sur une règle à suivre pour améliorer la robustesse d'un microcontrôleur. En revanche, il est maintenant évident que le réseau d'alimentation a un impact direct sur la robustesse d'un microcontrôleur, car une modification des connections sur une même puce change complètement les résultats.

2 L'hypothèse de la conversion du mode commun vers le mode différentiel

La particularité du stress FTB est qu'il est appliqué en mode commun sur l'alimentation. Or, lorsque l'on applique une perturbation en mode commun, la masse et l'alimentation ont la même variation. Si tel est le cas, le circuit soumis à une telle perturbation ne voit pas son alimentation varier, car la différence de potentiel entre la masse et l'alimentation reste constante. Il n'est

donc théoriquement pas possible de perturber un circuit avec un stress en mode commun. Et pourtant, nous observons bien des défaillances lorsqu'un microcontrôleur est soumis au test FTB.

Un tel comportement du circuit amène directement à l'hypothèse suivante. Les circuits internes perçoivent un stress différentiel. Il y a donc une conversion du stress en mode commun vers un stress en mode différentiel. Comment un tel phénomène peut-il avoir lieu ?

Lorsque le réseau d'alimentation est considéré comme parfait, une telle conversion n'est effectivement pas possible. En revanche, si la résistance, l'inductance et la capacité parasite des conducteurs rentrent en jeu, la conversion devient possible. Prenons l'exemple simple d'un circuit alimenté par deux fils : un fil de masse et un fil d'alimentation. Prenons en compte la résistance, l'inductance et la capacité parasite de ces fils par rapport à une masse parfaite. Chaque fil peut être considéré comme un filtre RLC, avec sa propre fréquence de coupure. Ainsi, si l'on applique le même signal à l'entrée d'un des deux fils, à une fréquence suffisamment élevée, le signal à la sortie du fil devient différent de celui appliqué à son entrée. Si les deux fils ont des paramètres RLC différents, à une fréquence suffisamment élevée, la sortie du fil de masse, est donc différente de la sortie du fil d'alimentation. Un signal identique appliqué à l'entrée des deux fils (en mode commun) donne donc une différence de potentiel à la sortie. La perturbation s'est donc convertie du mode commun vers le mode différentiel.

Cette hypothèse implique donc de prendre en compte les paramètres de résistance, d'inductance et de capacité du réseau d'alimentation, mais également une perturbation dans un domaine de fréquences suffisamment élevées pour que ces paramètres aient une influence significative.

3 Les gros contributeurs de la conversion mode commun vers mode différentiel

L'hypothèse développée dans la partie précédente suppose que la conversion du mode commun vers le mode différentiel est la cause des défaillances au test FTB. Ce phénomène est dû à la dissymétrie entre la masse et l'alimentation dans le réseau. Ce phénomène n'est significatif qu'à partir d'une certaine fréquence, celle-ci dépendant de l'ordre de grandeur des paramètres RLC du réseau. L'étude des principaux paramètres RLC du réseau d'alimentation d'un microcontrôleur, dans la configuration du test FTB fait l'objet de cette partie.

Pour cette étude, le banc de test a été découpé en quatre parties :

- La puce, qui contient uniquement le silicium
- le package
- le PCB (Printed Circuit Board)
- le banc de test, qui contient les câbles d'alimentation.

Le générateur de stress et la pince de couplage sont considérés comme parfaits.

En suivant le chemin du stress, le premier élément rencontré est la partie dite « banc de test ». Celle-ci contient un câble de masse et un câble d'alimentation qui relient la pince de couplage au PCB. Chacun de ces câbles est coupé et soudé à la main, et fait environ 10cm. Le paramètre prépondérant de ces fils est leur inductance. La dissymétrie est due à la manipulation à la main sans précaution particulière.

Ensuite vient le PCB. Il est conçu de manière à avoir un plan de masse et un plan d'alimentation. Chacun de ces plans a une capacité par rapport à la masse parfaite du banc de test (la table sur laquelle sont posés les éléments), mais aussi une capacité l'un par rapport à l'autre. Sur le PCB, prennent également place les pistes qui connectent les plans d'alimentation au boitier. Le nombre de pistes dépend du nombre de pattes d'alimentation à connecter, et la longueur de leur emplacement autour du boitier. Pour le PCB, les éléments

principaux sont donc les capacités et les inductances des pistes de connections. Ils sont non négligeables et ils engendrent des dissymétries entre la masse et l'alimentation.

En série avec les pistes du PCB, on retrouve la connectique entre le PCB, le boitier et la puce. Ici, les fils étant très proches, l'inductance mutuelle a un effet non négligeable sur ces connexions. Les paramètres principaux restent tout de même l'inductance, avec une dissymétrie due aux nombre de connexions ainsi qu'à leur placement dans le boitier.

A l'intérieur du boitier, se trouve la puce contenant un réseau d'alimentation complexe. Dans ce réseau, seul un anneau, faisant la périphérie de la puce, est connecté directement au boitier. Le reste de l'alimentation se situe en aval d'un régulateur de tension et ne sera pas pris en compte dans cette étude. Nous allons donc uniquement étudier, ici, les paramètres de l'anneau. Cet anneau est inductif et résistif avec un ordre de grandeur de 1 Ohm par millimètre. La résistivité de l'anneau est importante comparée aux paramètres de résistance rencontrés précédemment. Les réseaux de masse et d'alimentation de la puce ont également une capacité par rapport au plan de masse parfait du banc de test.

Lorsque l'on effectue la simulation avec un modèle simpliste, créé à partir des ordres de grandeur déterminés précédemment, il apparait que le mode commun se transforme de manière significative en mode différentiel autour de la centaine de MégaHertz. Si l'on compare ce résultat au spectre du stress FTB, nous démontrons qu'une telle conversion, du mode commun vers le mode différentiel, se produit lorsque le microcontrôleur est soumis au test FTB.

4 Conclusion

La perturbation FTB est appliquée en mode commun sur l'alimentation des microcontrôleurs. Une telle perturbation ne peut pas perturber un circuit électronique si elle ne se convertit pas en stress différentiel. Le mécanisme d'une telle transformation a été expliqué. Il a été démontré que, lors du test FTB, les

conditions de la conversion du stress en mode commun vers le mode différentiel sont réunies.

Chapitre 3 Méthodes d'analyse du réseau d'alimentation

1 Le comportement du réseau d'alimentation

La réponse en mode différentiel d'un réseau d'alimentation simple, composé de deux fils, à un stress de type FTB en mode commun, contient des phénomènes de résonance facilement observables en simulation. Ces phénomènes de résonance amplifient la conversion du stress en mode commun vers le mode différentiel. La mesure étant extrêmement difficile pendant un stress FTB, comment peut-on connaître la réponse réelle du réseau d'alimentation ?

1.1 Mesure de la réponse impulsionnelle

Considérons la réponse au stress comme étant la réponse impulsionnelle du réseau, dans la plage de fréquence excitée par le stress, et le réseau comme étant linéaire et invariant. Il est donc également possible de balayer le spectre de fréquence avec une sinusoïde à l'entrée du réseau et de mesurer, pour chaque fréquence, la valeur de l'amplitude en sortie. Le rapport des deux permet de connaître la réponse impulsionnelle. En revanche, dans le cas d'un microcontrôleur, la sortie étant l'alimentation des circuits sur le silicium à l'intérieur du boitier, elle est inaccessible.

La résonance d'un circuit RLC correspond à un pic de tension, et de courant. Ainsi elle correspond également à un pic de rayonnement électromagnétique. Or, il existe des outils, utilisés dans le domaine de la CEM,

qui permettent de mesurer le rayonnement électromagnétique d'un microcontrôleur. De cette manière, il est possible d'observer une image de la réponse impulsionnelle du réseau d'alimentation, en l'excitant avec une sinusoïde et en mesurant son rayonnement électromagnétique.

2 Méthodes d'analyse de résonance

2.1 Analyse de résonance globale

Deux méthodes d'analyse du réseau d'alimentation ont été développées en partant du principe décrit ci-dessus. Pour ces deux méthodes, une cellule TEM est utilisée pour mesurer le champ électromagnétique émis par le réseau d'alimentation lorsqu'il est excité par un générateur de sinusoïde. Un analyseur de spectre mesure la sortie de la cellule TEM.

La première méthode consiste à injecter la sinusoïde en mode différentiel entre la masse et l'alimentation. Ce n'est pas la méthode la plus proche du banc de test FTB, mais elle permet d'utiliser la cellule TEM de manière normale. Cette méthode permet d'extraire un spectre de résonance du microcontrôleur.

Une deuxième méthode permet d'injecter le signal en mode commun sur l'alimentation et la masse du microcontrôleur. Cette fois ci, le PCB est isolé de la cellule TEM par une entretoise. La cellule TEM mesure donc le champ électrique de mode commun qui vient perturber la mesure. Malgré cela, cette méthode reste plus proche de la configuration du test FTB.

2.2 Analyse de résonance locale

Les deux méthodes précédemment décrites mesurent le champ émis par le réseau d'alimentation de manière globale. Ceci suppose que l'amplitude soit homogène dans le réseau d'alimentation. Or, nous pouvons montrer, en simulant un simple réseau RLC avec plusieurs étages en cascade, que l'amplitude diffère à chaque jonction. Le réseau d'alimentation du

microcontrôleur étant bien plus complexe, deux autres méthodes d'analyse ont été développées pour mesurer l'amplitude locale.

L'une, dite par émission conduite, utilise un banc de mesure existant de la CEM [36] pour mesurer l'amplitude de la variation de tension tout autour de la puce. Les entrées/sorties, connectées le long de l'anneau d'alimentation interne, sont utilisées en sortie afin d'observer la valeur d'un « 1 » logique qui est à l'image de l'alimentation en son point. De cette manière, il est possible de dresser, autour de la puce, une cartographie de l'amplitude de la variation sur l'alimentation. La même chose peut être faite avec la masse.

L'autre méthode utilise un banc de mesure de champ proche pour cartographier le champ émis par le réseau d'alimentation. Une sonde de champ électrique ou magnétique est déplacée au-dessus du microcontrôleur grâce à une table numérique. Dans le même temps, une sinusoïde est appliquée sur son alimentation. De cette manière, il est possible d'établir une cartographie du champ émis par la puce.

2.3 Circuit de mesure embarqué

Une dernière méthode complètement différente a été abordée durant ce travail de thèse. Il s'agit d'un circuit de mesure embarqué. Ce circuit peut mesurer sa propre alimentation et est suffisamment rapide pour capturer des temps de montée de l'ordre de quelques nanosecondes. Son principe a été validé sur puce de test en technologie 40nm. Ce circuit étant embarqué, il nécessite de créer des microcontrôleurs embarquant cette solution. Nous avons préféré nous focaliser sur les méthodes non intrusives décrites précédemment.

3 Conclusion

Quatre méthodes d'analyse du réseau d'alimentation ont été développées dans ce chapitre. Chacune possède ses avantages et inconvénients. Ces outils sont également complémentaires les uns des autres. Ainsi il est

possible de choisir la méthode approprié à nos besoins selon la précision, le coût, ou la difficulté de mise en œuvre.

Chapitre 4 Application à l'amélioration de la robustesse et perspectives

Ce dernier chapitre est destiné à montrer l'apport de ce travail de thèse sur la compréhension des mécanismes du test FTB et sur les ouvertures pour améliorer la robustesse des produits.

1 La modification des paramètres extérieurs du réseau d'alimentation change le seuil de robustesse

Sur deux microcontrôleurs, CHIP1 et CHIP2, différents mais très proches en termes de conception et suivant le même flot de fabrication, nous avons modifié certaines parties du réseau d'alimentation sans modification du silicium.

1.1 Des résultats contradictoires

Il s'avère qu'une même modification dans les deux cas ne change pas les seuils de robustesse dans le même sens. En effet, si l'on prend pour exemple l'ajout d'un plan de masse à l'intérieur du boitier, la robustesse du CHIP1 est améliorée, alors qu'elle est dégradée pour le CHIP2. Devant un tel résultat, le plan de masse en tant que piste d'amélioration de la robustesse est considéré comme impossible car trop aléatoire.

1.2 Retrouver la cohérence grâce aux outils d'analyse

Maintenant, lorsque nous regardons le résultat de l'analyse de résonance global en mode différentiel, nous nous apercevons que dans les deux cas, la première résonance est décalée vers les hautes fréquences quand nous ajoutons un plan de masse dans le boîtier. Les outils d'analyse et la compréhension de l'importance des phénomènes de résonance dans la conversion du stress du mode commun vers le mode différentiel permettent de donner une cohérence entre les deux cas.

1.3 Détermination d'une zone de faiblesse

Si l'on pousse l'analyse plus loin et que l'on modifie la première fréquence de résonance de chacun des microcontrôleurs de différentes manières (modification du nombre d'alimentations, modification du PCB et du boîtier), nous nous apercevons que pour chaque modification de la fréquence de résonance, il y a un seuil de robustesse différent. De plus, si l'on superpose les résultats d'analyse de résonance de chacune des puces, nous voyons apparaitre une zone fréquentielle de faiblesse. En effet, il y a une bande de fréquence dans laquelle une résonance donne un seuil de robustesse plus bas. Lorsque la première fréquence de résonance s'éloigne de la zone de faiblesse, le seuil de robustesse remonte.

Si l'on revient au cas du plan de masse dans le boîtier appliqué au CHIP1 et au CHIP2, l'ajout du plan de masse sur CHIP1 éloigne la résonance de sa zone de faiblesse, et améliore ainsi ses résultats. C'est l'inverse pour le CHIP2. Ainsi, les résultats semblaient contradictoires.

2 Conclusion

Ce travail de thèse a permis d'obtenir les clés pour comprendre les mécanismes de propagation du stress FTB. Cette compréhension a permis de fournir des outils d'analyse du réseau d'alimentation. L'un de ces outils

d'analyse a été exploité dans ce dernier chapitre afin de trouver une piste d'amélioration de la robustesse d'un microcontrôleur avec l'identification d'une zone de faiblesse fréquentielle. Cependant, tout le potentiel de ce travail de thèse n'a pas encore été exploité.

3 Perspectives

Les autres outils développés dans le troisième chapitre ont été validés, mais non exploités à des fins d'amélioration des microcontrôleurs. Ils pourraient être utilisés, par exemple, pour établir un flot d'identification des défaillances.

L'étude menée dans le dernier chapitre a permis d'identifier une zone de faiblesse fréquentielle. Actuellement, aucun moyen de placer la première résonance hors de cette zone de manière prévisible n'a été développé.

La modélisation du réseau d'alimentation, à l'étape de conception, pourrait également être d'un grand intérêt pour créer des microcontrôleurs robustes. En effet, ceci permettrait de simuler les circuits, en y appliquant un modèle de stress FTB, et ainsi faire des circuits robustes, ou bien de créer des versions de boîtier évitant une résonance dans la zone de faiblesse.

Conclusion générale

A travers ces 4 chapitres, ce travail de thèse donne les clés pour comprendre et analyser les défaillances des microcontrôleurs au test FTB. Alors que les perturbations en mode commun pouvaient sembler inoffensives, leur transformation en mode différentielle par le réseau d'alimentation les rend dangereuses. En effet, les éléments parasites du réseau tel que : les résistances, les inductances, et les capacités introduisent une dissymétrie entre le potentiel de référence et l'alimentation. Le spectre fréquentiel de la perturbation rend également cette transformation significative.

Le réseau d'alimentations est un réseau RLC complexe résonnant. Cette particularité a été exploitée afin de développer des outils d'analyse de ce réseau. Ces méthodes utilisent le rayonnement électromagnétique du réseau afin d'en extraire son spectre de résonance.

Les outils développés dans ce travail de thèse ont ensuite été utilisés afin d'améliorer la robustesse des microcontrôleurs. Il a été montré qu'il est possible d'améliorer les performances d'un microcontrôleur par simple modification de son boitier, ou du PCB sur lequel il est implémenté, et ce, grâce au spectre de résonance.

Ceci est seulement un exemple de ce qui peut être réalisé grâce à ces travaux. Un large champ de perspective est ouvert, que ce soit en termes d'investigation ou d'amélioration des produits. Ils donnent également les clés pour élaborer un model afin d'effectuer des simulations en amont.

Appendix B: Publications

National

“ Influence du nombre d’alimentations sur la susceptibilité des microcontrôleurs aux essais d’immunité aux transitoires électriques rapides en salves.”
Yann Bacher; Cesar Gori; Nicolas Froidevaux; Philippe Dupre; Henri Braquet; Gilles Jacquemod
2014 Journées Nationales du Réseau Doctroral en Micro-Nanoélectronique

International

“ Supply network setup impact on fast transient burst test in microcontrollers”
Yann Bacher; Cesar Gori; Nicolas Froidevaux; Philippe Dupre; Henri Braquet; Gilles Jacquemod
2014 SAME (Sophia Antipolis Microelectronics Conference)

“Influence of supplies on fast transient burst test in microcontrollers”
Yann Bacher; Cesar Gori; Nicolas Froidevaux; Philippe Dupre; Henri Braquet; Gilles Jacquemod
2015 IEEE 6th Latin American Symposium on Circuits & Systems (LASCAS)
Pages: 1 - 4, DOI: 10.1109/LASCAS.2015.7250418

“A new RLC structure measurement method using a Transverse ElectroMagnetic cell”
Yann Bacher; Arnaud Gamet; Nicolas Froidevaux; Philippe Le Fevre; Henri Braquet; Gilles Jacquemod; Stéphane Meillère; Marc Bendahan
2015 IEEE International Circuits and Systems Symposium (ICSyS)
Pages: 7 - 10, DOI: 10.1109/CircuitsAndSystems.2015.7394054

“Resonance analysis for EMC improvement in integrated circuits”
Yann Bacher; Nicolas Froidevaux; Philippe Dupre; Henri Braquet; Gilles Jacquemod
2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)
Pages: 56 - 60, DOI: 10.1109/EMCCompo.2015.7358330

Etude et modélisation des perturbations produites au sein des microcontrôleurs STM32 soumis à des stress en impulsion

La fiabilité des microcontrôleurs est cruciale compte tenu de leur utilisation massivedans de nombreux domaines, surtout dans des environnements sévères. De ce fait, larobustesse aux perturbations électromagnétiques, en particulier à propos desalimentations, est un axe de développement majeur, que ce soit pour acquérir unavantage comparatif sur le marché, ou simplement pour assurer la sécurité des bienset des personnes. En ce sens, nous avons étudié le test de ces circuits soumis à desagressions transitoires rapides en salve définies par la norme IEC 61000-4-4. Lesmécanismes spécifiques de propagation de la perturbation en mode commun sontmis en évidence, ainsi que leur conversion en mode différentiel. Plusieurs méthodesde mesure, dont certaines originales, ont été développées pour valider cetteconversion, ainsi que les modes de propagation. Sur cette base, le réseau dedistribution des alimentations a été particulièrement étudié et son influence sur larobustesse du circuit a été mise en évidence. Enfin, cette thèse ouvre de nouvellesperspectives d'amélioration de la robustesse des microcontrôleurs et des circuitsintégrés en général, pour ce type d'agression, et donc de leur fiabilité.

Study and modelling of the disturbances produced within the STM32 microcontrollers under pulsed stresses

The reliability of the microcontrollers is crucial considering their massive use innumerous domains, especially in severe environments. Therefore, the robustness inthe electromagnetic disturbances, in particular for the power supply network, is amajor development, whether it is to acquire a comparative advantage on the market,or simply to assure the goods and people safety. Therefore, we studied the FastTransient Burst test of integrated circuits, as defined by the IEC 61000-4-4 standard.The specific propagation mechanisms of the disturbance in common mode arehighlighted, as well as their conversion in differential mode. Several measurementsmethods, among which certain novel, were developed to validate this conversion, aswell as the propagation modes. Based on this, the power distribution network wasparticularly studied and its influence on the robustness of the circuit washighlighted. Finally, this work opens new perspectives of improvement of themicrocontrollers' robustness, for this kind of aggression, and thus their reliability.